CPTR-380
Exam 2 planning

Exam 2 will emphasize material from chapters 4 and 5 of the text.

Chapter 4 starts with describing the various datapath elements such as memory, PC, adders, registers, ALU, etc. You are expected to be knowledgeable about those. The clocking methodology described on pages 261 & 262 should be understood as it is foundational for understanding pipelining. You should still know the R, I, and J MIPS instruction formats.

You should understand the single cycle datapath since it forms a basis of understanding instruction execution and pipelining. However, questions from chapter 4 will focus most on pipelining: how it works and its challenges.

Understand how a pipeline works.

Know and understand pipeline hazards: structural, data, control. Be able to identify where in a sequence of machine instructions a data hazard would occur and how data hazards are mitigated with forwarding. Know how circuitry is arranged to implement forwarding. Likewise, be able to identify a control hazard in an instruction sequence and if a stall is needed how that is implemented in hardware. Be knowledgeable regarding how control signals generated in the ID stage of the pipeline for a particular instruction follow along with the data of that instruction in successive pipeline stages. How is instruction flushing done when needed?

Be aware of how an exception is handled & the hardware needed to implement that.

We spent little time on instruction level parallelism (section 4.11) so no questions on that.

Questions from chapter 5 will emphasize the concept of memory hierarchy and specifically caching. Have a general idea of relative access speeds (access times) for registers, level 1 cache, main memory, disks. Understand direct, set associative, fully associative mapping. Know how a block is found in cache, how choices may be made to replace a block Understand terms such as hit, miss, dirty bit, valid bit, and how they are used.

Regarding virtual memory, less depth of knowledge, but you should understand what is described in figures 5.24. 5.25, 5.26, 5.27