ENGR-354
Exam 2 planning

The first exam focused on boolean algebra, truth tables, logic reduction using boolean algebra and regular K-maps and a little on using entered variable K-maps. These are basic tools used often in analyzing and designing logic circuits. So while they are not directly the topics of concern on exam 2 they may be needed to properly do a solution on exam 2.

The emphasis of exam 2 will be topics covered since exam 1. These include:

- decoders such as 2:4 or 3:8 binary decoders
- multiplexers such as 2:1, 4:1
- adder such as a one-bit half adder or one-bit full adder
- basic cell (simple memory circuit)
  NAND centered (i.e. constructed with NAND gates), set dominant
  NOR centered, reset dominant
- D-latch, transparent memory
- D flip-flop (the term flip-flop is used when the clock input is edge triggered)
- State machine
  - consists of next-state logic, memory, and output logic circuit blocks
- State diagram, used to document the operation of a state machine
  - consists of states, state numbers, branches between states, branching conditions, outputs
  - shows branching conditions required to transition from one state to another
  - shows the sequence of possible state-to-state transitions
  - shows when outputs are asserted in each state.
- Branching condition rules, two of them - VERY important:
  - Sum rule. The sum (logic OR) of branches out of a state must equal logic '1'
  - Uniqueness. Branching conditions for each branch out of a state must be unique.
- Next state logic design; given a state diagram on which state numbers have been assigned, be able to create minimized next state logic; be able to create output logic
  - The next state depends on what the present state is and what the input signals are. Next state logic creation depends on this and also on the type of memory used for the state machine. Thus what we call the excitation table of the memory is important. That just means knowing how the input to memory needs to be asserted to cause a transition from one memory state to another. We usually use D flip-flops as memory and the associated D-F/F excitation table.

While the exam is not yet written, I expect there to be problems such as:

- Using a decoder or mux, implement a combinatorial logic function
- Find next state logic given a state diagram with 2, 3, or 4 states
- Find output logic given a state diagram
- Determine if branching conditions are met given a state diagram
- Create a new flip-flop or latch given its function table
- Possibly, analyze a given circuit for its output sequence or state sequence

For review, the parts of a state diagram: