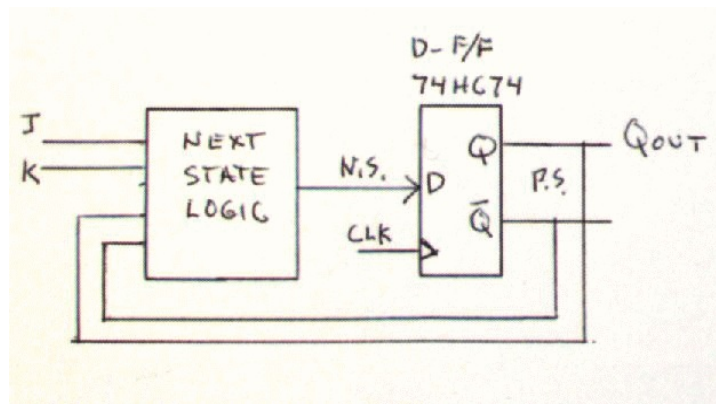
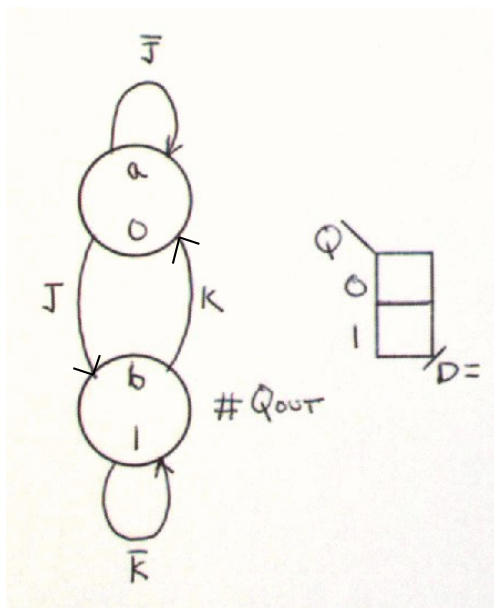


ENGR-354
HW#14

- 1) Below is the state diagram for a JK flip-flop and a block diagram for a state machine to create an edge triggered JK flip-flop using a D flip-flop as the memory. After designing the circuit wire up the circuit on your bread board and test.
 - a) Design the next state logic (i.e. find the equation for signal D)
 - b) Draw a logic circuit diagram
 - c) Refer to a document listed as “Logic part pin definitions, i.e. pinouts (pdf)” under a section heading of “Notes and useful information” on the class web page to find components that contain the type of logic gate you wish to use. Recall that there are NAND and NOR gates with 2 or 3 inputs but no AND and OR gates. The D flip-flop chip is a 74HC74 (SN74HC74 or MC74HC74 on the chip itself) and there are two flip-flops in each chip package.
 - c) Write the pin numbers of the chips you use on the inputs and outputs of components in your logic circuit diagram
 - d) Wire it up and test
 - e) Take a photo of your breadboard setup and submit as part of your homework (it can be submitted as a separate file if desired)

(Refer to HW#10 handout to refresh knowledge about hooking things up to the breadboard)

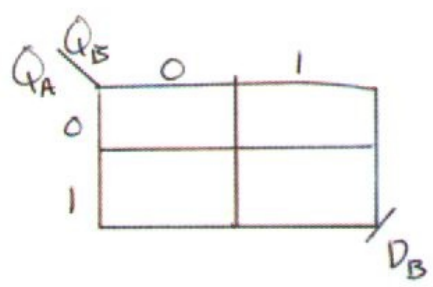
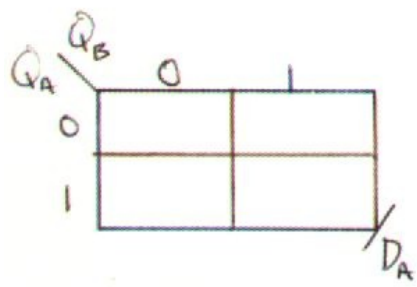
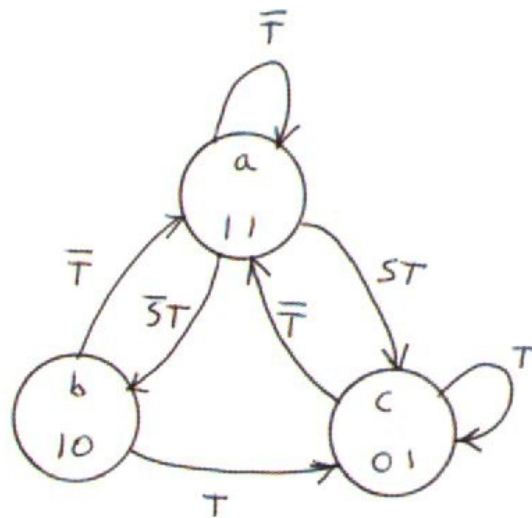
- Connect the J and K inputs of your circuit to two switch outputs of your logic interface board.
- Connect another switch output of the logic interface board to the clock input of the D flip-flop.
- Connect the Q output of the flip-flop to a logic interface board input and hence an LED
- Connect power and ground like was done in HW#10
- The D flip-flop has two inputs for clearing memory to zero or presetting memory to one (named PRE-bar and CLR-bar). These both need to be at a high voltage for the memory to work, so connect both of them to 3volts.



D F/F operation table

	D
0 ->	0 0
0 ->	1 1
1 ->	0 0
1 ->	1 1

- 2) Design the next state logic for the logic circuit whose operation is defined with the state diagram below. Just find the logic expressions for the next state logic. You don't need to draw the circuit.



Submit homework to the D2L drop box