ENGR-354
HW # 15

1) The operation table for a possibly unusual (perhaps nonsense) flip-flop with two inputs L and N is shown below.
   a) Create the two-state state diagram for this flip-flop
   b) Using an edge triggered D flip-flop as memory, create next-state logic for this flip-flop.
   c) Implement the circuit, i.e. draw a logic diagram for this circuit

L	N	Q_{t+1}
0	0	1
0	1	Q_t
1	0	$Qbar_t$
1	1	0

2) State machines sometimes are handy for generating a sequence of desired signals accurately turned on or off relative to other signals. Below is a timing diagram that shows two signals Pout and Zout that need to be repeatedly asserted for one or more clock cycles (note that they are asserted for one clock cycle or a multiple of clock cycles). In this simple case there is no start or stop signals, the circuit just repeatedly creates the shown signals. With no holding branches, at each rising edge of clock there is a transition to a new state.

   a) Label the state diagram with outputs
   b) Create next-state logic for this state machine assuming rising edge triggered D flip-flops are used for state machine memory (show your work)
   c) Create output logic for this circuit
   d) Implement the circuit, i.e. draw a logic diagram for the circuit.