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-- Engr 433  Example of a hierarchical design written in one file.
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--   This example implements the SOP xor function  F =  A'B + AB'
--     by defining AND and OR gates and then top level called myxor.

Library ieee;
Use ieee.std_logic_1164.all;

Entity myAnd is
   port(a,b : IN std_logic;
          f : OUT std_logic);
End myAnd;

Architecture myAndFunc Of myAnd is
Begin
  f <= ((NOT a) AND b);
End myAndFunc;

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Library ieee;
Use ieee.std_logic_1164.all;

Entity myOr is
   port(c,d : IN std_logic;
          g  : OUT std_logic);
End myOr;

Architecture myOrFunc Of myOr is
Begin
   g <= (c OR d);
End myOrFunc;

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Library ieee;
Use ieee.std_logic_1164.all;

Entity myXor is
   port(x,y : IN std_logic;
          h : OUT std_logic);
End myXor;

Architecture myXorStruct Of myXor is
   Signal C1,C2: Std_logic;
   Component myAnd
      port(a,b : IN std_logic;
             f : OUT std_logic);
   End Component;
   Component myOr
      port(c,d : IN std_logic;
             g : OUT std_logic);
   End Component;
Begin
   gate1: myAnd Port Map (x,y,C1);
   gate2: myAnd Port Map (y,x,C2);
   gate3: myOr  Port Map (C1,C2,h);
End myXorStruct;
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