ENGR-433
HW # 7

1) Draw and label a conceptual diagram showing the functional parts and their interconnection defined by this section of VHDL description:

```
signal clk_next, clk_reg : unsigned(9 downto 0);
signal aclk, slowclk : std_logic;

process(mclk)
begin
     if (mclk'event and mclk='1') then
          clk_reg <= clk_next;
end if;
end process;
clk_next <= (others=>'0') when clk_reg=999 else clk_reg+1;
aclk <= '1' when clk_reg < 500 else '0';
Clk_Buffer: BUFG port map ( I => aclk, O => slowclk);
```

2) Assume that a 6-bit free-running counter is needed (free-running means that when the count reaches maximum for an up counter, on the next clock tick it goes to back zero without any detection circuits, or if counting down, when it reaches zero then on the next clock tick it goes to its maximum count and decrements from there). In addition to clock, assume the counter has one control signal. When the control signal is a logic ‘1' it counts up and when logic ‘0' it counts down.
   a) Draw a conceptual diagram of a circuit to do this.
   b) Write VHDL statements to implement this (you don’t need to write entity and architecture statements, just the statements that define the counter, like in problem 1 above). And like in problem 1 above, you can use arithmetic operators in the VHDL.