Lab Exercise #2

Objectives

- Gain further experience designing digital circuits
- Design a circuit that counts events and uses counters to derive needed clock signals
- Use an FPGA to implement the design

References

Notes for schematic driven design (pdf) on the class web page
Configuration file on class web page showing pinouts
Xilinx documents on the class web page.

Lab 2 Problem Statement

A timer is needed to measure the time between a first and second pressing of a push button activated by a person's finger. Time is to be counted in 100ths of seconds up to 99. Switch bounce occurring in the first 10 milliseconds after the button is pressed should be ignored. If the time between first button press and second button press is equal to or greater than 990 milliseconds, the error light (LED15) will come on remain on until reset is pressed. When a proper time interval has been measured, i.e. one that is less than 1000 ms, the number of 100ths of a second will be displayed using 8 LEDs in BCD (binary coded decimal) notation. Pressing reset will set the circuit up to again look for a button press.

A state machine must be used to monitor button presses (which are inputs to state machine), start time counting when the button is pressed, and determine if the time allowed time interval is exceeded.

Specific input/output resources to use:

sw11 will be the button that the user presses twice
sw9 will be the reset button
led3 down to led0 will be the right hand digit of the measured time
led7 down to led4 will be the left hand digit of the measured time
led15 will be the error light indicating more than 990 milliseconds between presses of sw11

The Xilinx library for schematic driven design contains D flip-flops, D latches, counters, many types of AND, OR, NAND, NOR, XOR gates with various numbers of inputs, 2:1 mux, 4:1 mux, 8:1 mux, 2:4 decoder, 3:8 decoder, etc.

Extra: Make the error light flash on/off at a 5 flashes per second rate when time is exceeded using the same state machine that sees button presses and determines that time is up and that the light should turn on.

Design Flow

The general design flow for today's lab is:

- Design a circuit per the problem statement.
  Confirm understanding of the problem & partition the design into subsystems.
  Create a system block diagram
  Determine the signals needed into and out of the state machine
  Create a fully labeled state diagram. Use one-hot encoding of the state number
  Create logic functions for the next-state and output logic
  From the Xilinx library, find F/F's, counters, multiplexers, etc and understand their operation.
- Create a schematic for your design using the Xilinx schematic tool
- Synthesize an FPGA implementation (Place, route, and create a bit map file)
- Download bit map file to the FPGA board
- Test (debug if needed)

To Turn In

- By next lab period, a short report.
  While this report will be quite short, there must be an abstract, a paragraph about the lab project (a person reading an abstract should be able to learn what the problem was, the general approach taken to solve it, the solution, and the results or outcome). In addition to the abstract, include your block diagram, schematic (print-out from Xilinx), design notes, discussion of any problems encountered, and anything else you wish to include.

  Again, an abstract is concise (therefore short) and to the point.