ENGR-433
Further notes regarding lab 5

The lab 5 handout has a block diagram of the circuit expected for lab 5. During lab I gave further information on some of the blocks. I want to clarify details of the blocks.

Implementation strategy:
    I recommend developing the circuit without the multiplier by connecting the 8 switch inputs directly to the bin2bcd_module. That way the number going through the system is clearly known. Once the rest of the system is working then install the multiply module.

Multiplier block:
    Can come quite directly from lab 4. You can use it as a component or copy it into your top level VHDL file.

bin2bcd_module:
    Supplied. See class web page. You can use it as a component.

bin2_7seg:
    Supplied. See class web page. You can use it as a component.

clock_gen:
    VHDL is supplied as a text file on the class web page. Copy into your top level VHDL file (it has been updated to create a higher clock rate. See the Challenges item below)

2bit_counter
    VHDL is supplied as a text file on the class web page. Copy into your top level VHDL file

multiplexer
    Yours to write. Listing 4.5 page on 85 in the textbook is a good example.
    Write its description in your top level VHDL file. (you can create it as a component if you wish, but that is not required. Easiest just to place its description in your top VHDL file)

2:4 decoder
    Yours to write. Listing 4.6 page on 86 in the textbook is a good example.
    Write its description in your top level VHDL file. (you can create it as a component if you wish, but that is not required)

Challenges:
    When I tested the circuit with the supplied modules and descriptions I discovered that the 2bit_counter was not counting as desired. I expect it to cycle through 4 states that are encoded with two bits meaning its output should go 00, 01, 10, 11 and then start over. However, depending on the speed of the clock supplied to the counter this sequence may not be followed. On the following pages is proof. I don't know why at slower clock rates the 2bit counter doesn't count right. Running at 50Khz works ok and the display still responds ok. The following pages document what I found. I have not found an explanation.

FPGA mystery

Here is a VHDL description of a 2-bit counter:
Clock is derived from the 50Mhz clock and placed on an internal clock line with a BUFG

```
    signal cnt_next, cnt_reg : unsigned(1 downto 0);
    signal data_out : std_logic_vector(1 downto 0);

    process(clk)
    begin
        if (clk'event and clk='1') then
            cnt_reg <= cnt_next;
        end if;
    end process;
    cnt_next <= cnt_reg+1;
    data_out <= std_logic_vector(cnt_reg);

    extout7 <= data_out(0);
    extout8 <= data_out(1);
```
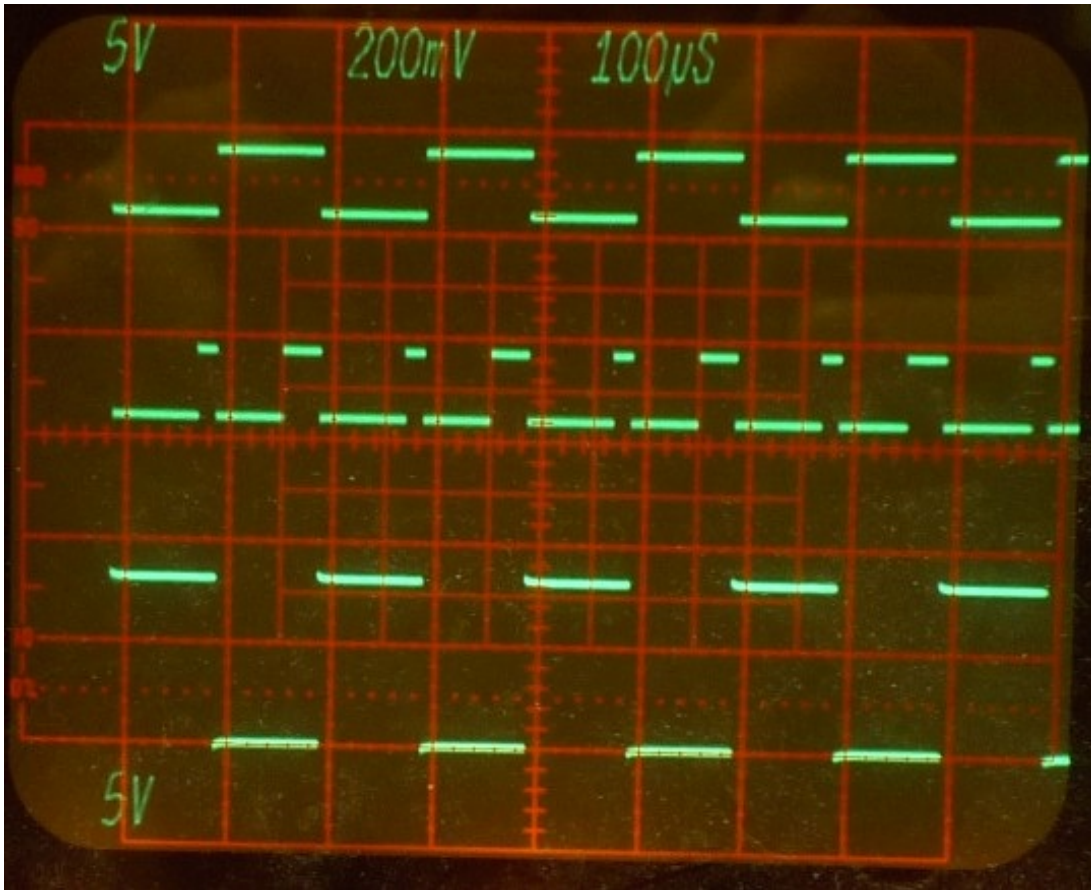
Waveforms in the pictures below are in this order:
    top -   data_out(1)   msb
    middle - data_out(0) lsb
    bottom - clock
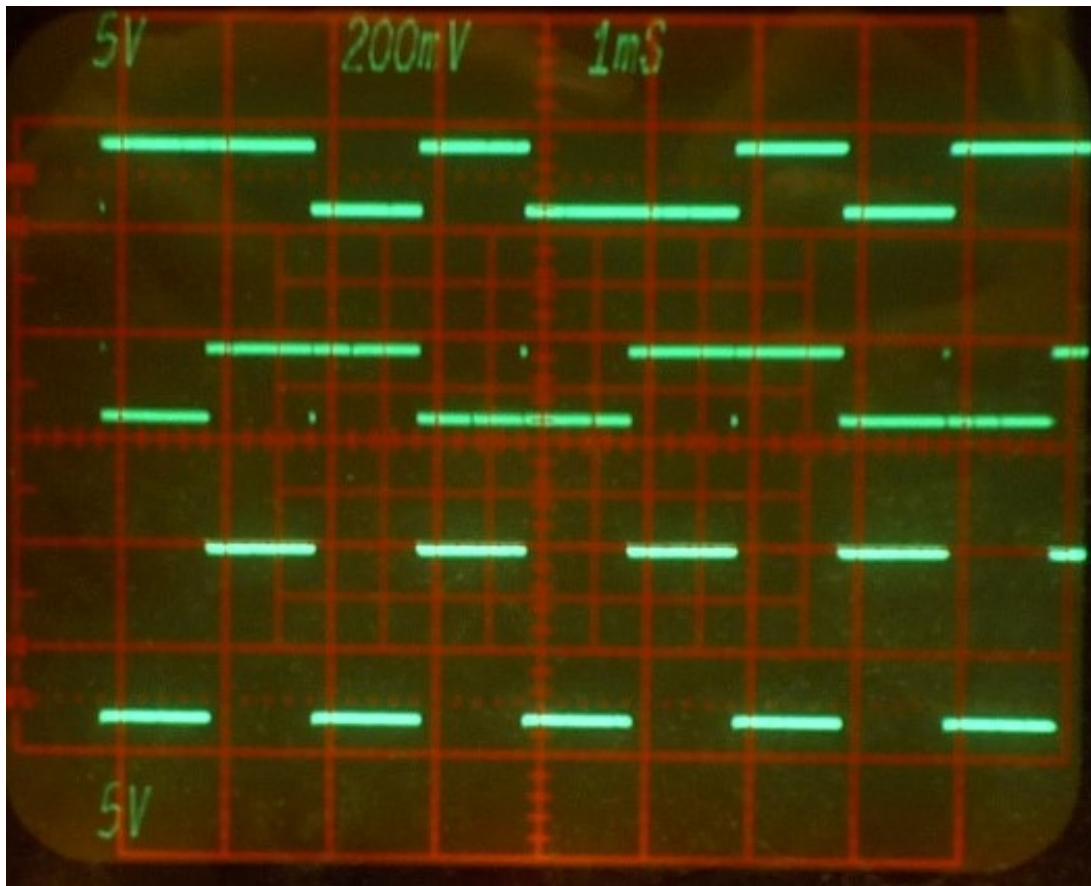   With a 50Khz clock, normal, expected waveforms
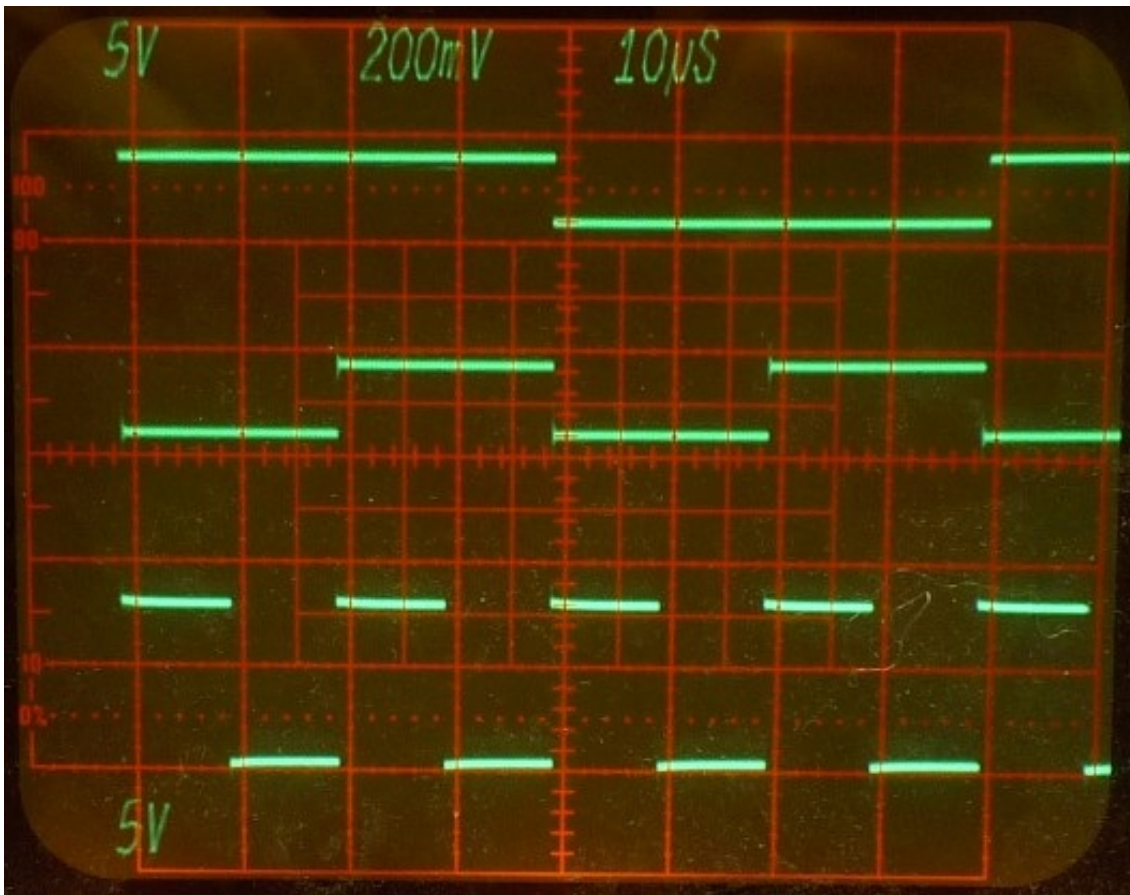
Waveforms with a 5Khz clock. Note transitions on data_out(0) other than on a clock edge.

Waveforms with a 500Hz clock:

Transitions are occurring on both clock edges. I have not found glitching on the clock signal when zoomed in (time zooming).