Timing Measurements With Fast Logic Circuits

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Abstract

This application report describes problems that can occur when making timing measurements with fast logic circuits. Introduction to methods of impedance matching and the determination of the impedance of a stripline are followed by the requirements for an efficient test setup. The report concludes with an example of such a test setup.

1 Introduction

The availability of ever-faster electronic components allows the design of more effective and efficient end equipment. However, this has led to increased problems from line reflections, resulting in signals having serious overshoot, undershoot, and steps on pulse edges.

When measuring the switching-time behavior of individual circuits, problems can arise with outputs having very steep edges, even under laboratory conditions. An appropriate test setup is the prerequisite for reliable, repeatable, and comparable measurement results. Essential conditions for a satisfactory test setup include:

- A stable power supply that also shows no voltage changes under conditions of varying high-frequency current
- An undistorted signal at the input of the device under test with no overshoots, undershoots, or steps on pulse edges
- A connection to the outputs of the device under test that does not influence the switching behavior
- Appropriate test equipment and knowledge of the influence of the equipment on the test setup

This report discusses problems and indicates possible solutions for timing measurements on individual devices.

2 Theory

If the rise and fall times of a signal are shorter than the signal transit time from the source to the end of the line, the designer must consider the resulting transient phenomena of voltage and current waves flowing forward and back along the line (see Figure 1). The signal waveform is determined by the:

- Internal resistance of the source (R_i)
- Characteristic impedance of the line (Z_L)
- Load resistance (R_L)
- Length of the line (L)

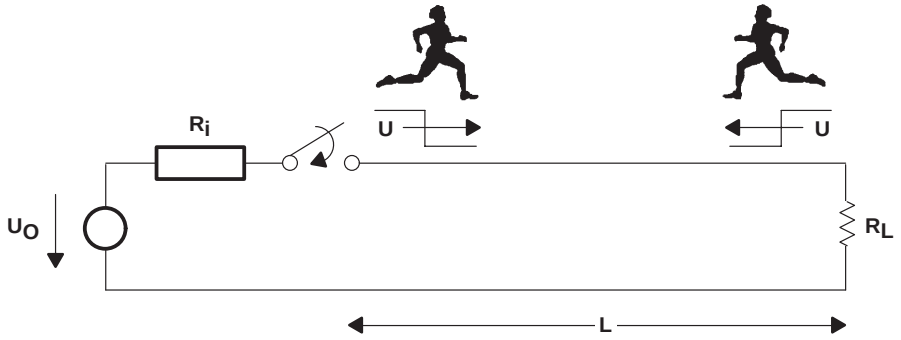


Figure 1. Wave Propagation Along a Line

2.1 Methods of Impedance Matching

Reflections of signals along an unterminated line cause overshoots, undershoots, or steps on pulse edges. Various methods of line matching are shown in Figure 2.

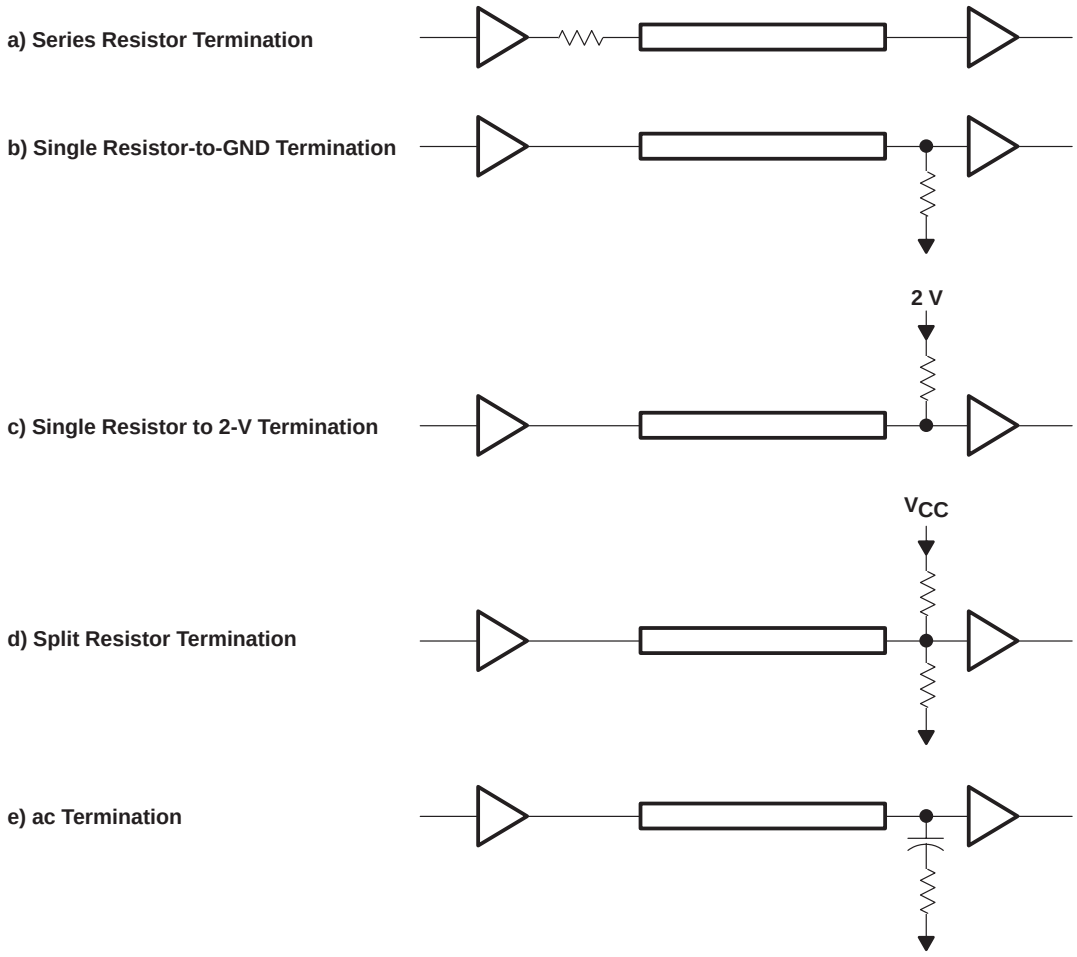


Figure 2. Methods of Line Matching

If the internal resistance of the source and the characteristic impedance of the line are matched exactly, no distortion of the waveform at the end of the line takes place (see Figure 2a). If the internal resistance of the source is less than the characteristic impedance of the line, a series resistor can be used for impedance matching. Although this method limits the drive capability of the source, it has the advantage that bidirectional channels can be realized without loading the output of the device under test when the source is in the high-impedance state.

If a value is chosen for the load resistor that is in accordance with the characteristic impedance, then line reflections will be eliminated (see Figure 2b). However, in this case, the signal source must have adequate capability to drive the relatively low resistance load. Many of the generators available on the market are already set to drive a particular terminating resistance, mostly 50 Ω. With such a generator, this method of line matching must be used; otherwise, the voltage level preset at the generator cannot be applied to the device under test. If a channel is operated bidirectionally during measurement, this method is not usable because the terminating impedance for the test device represents an unacceptable load.

If the dc current in the load resistance (and power consumption) needs to be reduced, the terminating resistance can be connected to a voltage other than 0 V, for example to 2 V (see Figure 2c). However, with this method, the voltage level at the input of the device under test will be determined by the voltage level of the source and, to a greater extent, by the voltage source of the line termination. In such a case, a precise test setup is no longer possible.

An additional option for matching the line is by using two resistors; the first is connected to 0 V and the second to V_{CC} (see Figure 2d). However, this method is not good practice for a test setup because the advantage of low dc current and power consumption is insignificant in this case; the resulting voltage level also depends on the source as well as on the supply voltage V_{CC}.

Another way of matching the line is to use a resistor and a capacitor in combination (see Figure 2e). In this case, the power consumption is reduced since the dc component is eliminated. The value of the capacitor can be estimated with the following equation:

$$R \times C > 4T \quad \textbf{(1)}$$

Where:

R = terminating resistor
C = terminating capacitor
T = signal propagation time from the beginning to the end of the line

The value of the capacitor needs to be chosen by trial and error so that when making a precise test setup, the type of line termination is not in question.

Signal generators commonly available are provided with an output resistor of 50 Ω, and the methods of line matching in Figures 2a and 2b can be chosen. The setting of the output voltage level is usually calibrated for a load resistor of 50 Ω, which is also the usual termination resistor of laboratory setups (see Figure 2b). The variation in Figure 2a is mainly applicable to production testing because, with it, bidirectional channels can be realized. The other three methods are not used for precise measurements in the laboratory.

2.2 Theoretical Voltage Waveforms

Using the Bergeron method, it is possible to theoretically determine waveforms on lines. The Bergeron method will not be explained here, but details can be found in the application report *The Bergeron Method*, literature number SDYA014.

Figures 3 through 8 show the voltage waveforms of a rising pulse at the beginning, in the middle, and at the end of a line. Falling pulses show similar behavior but with opposite polarities. The time of transit (T) of the signal from the beginning to the end of the line can be calculated using equation 4.

Figures show combinations of different series resistors without terminations (see Figures 3, 5, and 7) and with terminating resistors at the end of the line (see Figures 4, 6, and 8). Voltage waveforms with correctly terminated lines are shown in Figure 6; incorrect terminations are shown in Figures 3, 4, 5, 7, and 8.

The figures show that incorrect termination causes steps on the pulse edges or an overshoot of the signal. A line that is correctly matched with a series resistor delivers an undistorted waveform only at the end of the line; along the line there is a step on the pulse edge. Terminating the line with a load resistor ensures clean pulses along the entire length of the line.

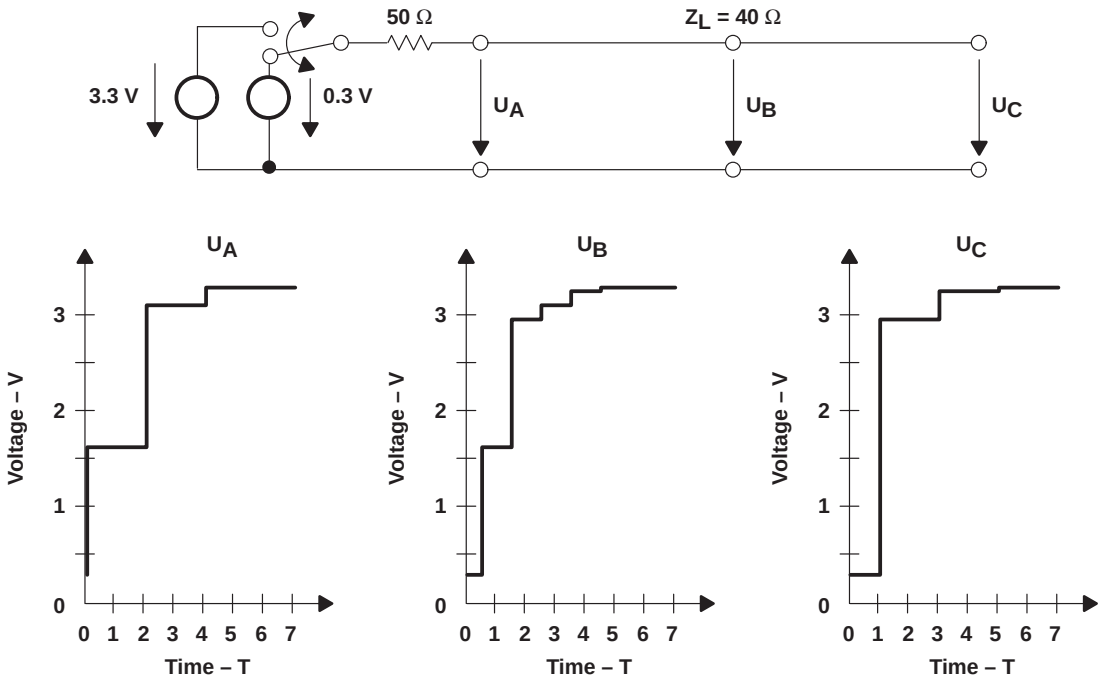


Figure 3. Voltage Waveforms With Incorrect Termination (Z_L = 40 Ω, No Terminating Resistor)

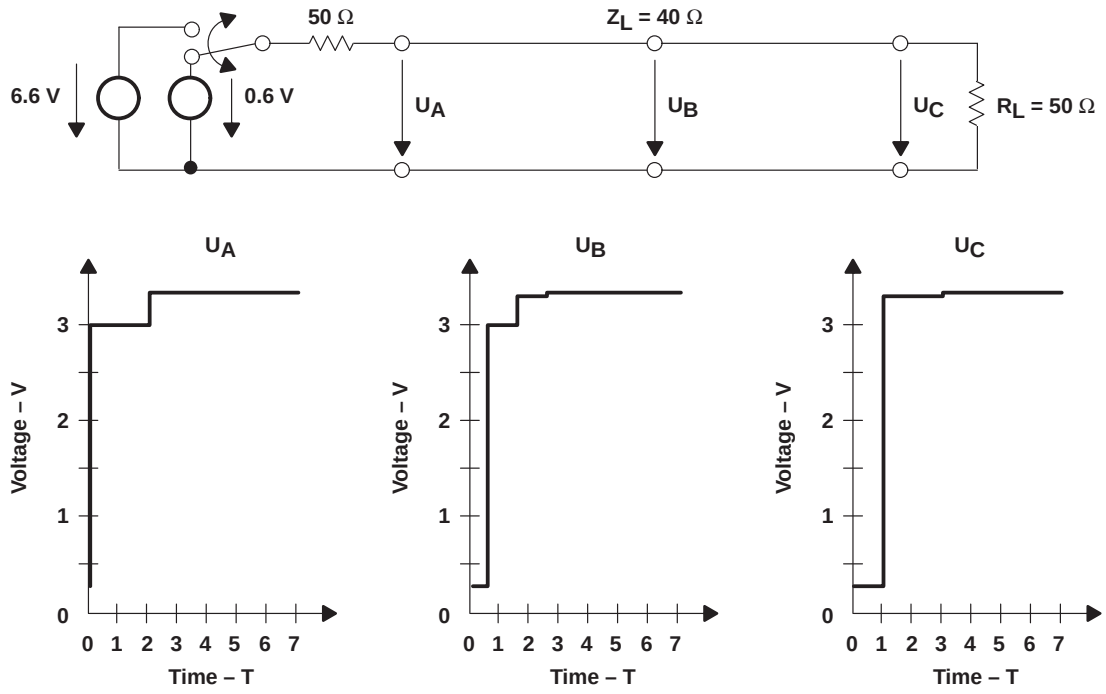


Figure 4. Voltage Waveforms With Incorrect Termination (Z_L = 40 Ω, Terminating Resistor of 50 Ω)

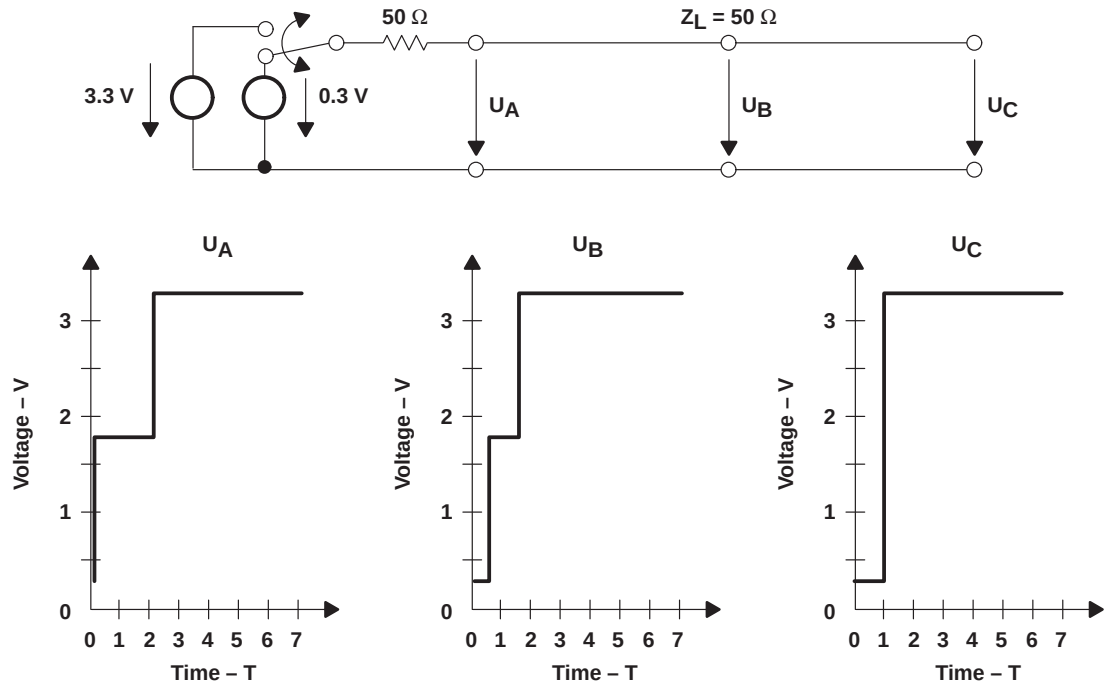


Figure 5. Voltage Waveforms With Impedance Matching (Z_L = 50 Ω, No Terminating Resistor)

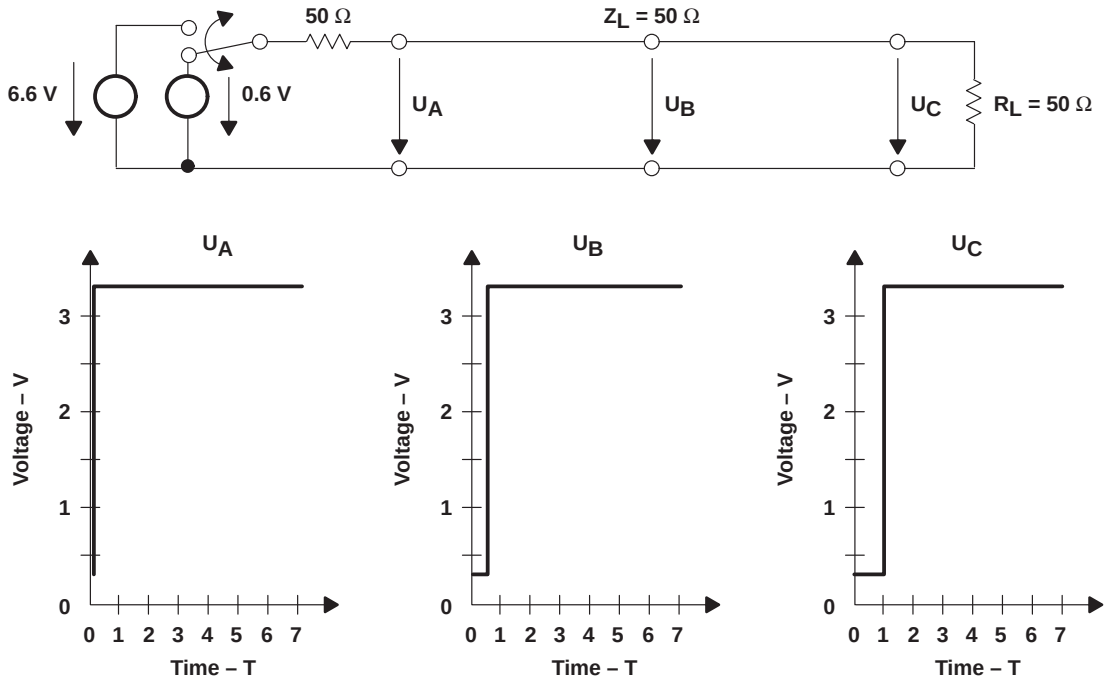


Figure 6. Voltage Waveforms With Impedance Matching (Z_L = 50 Ω, Terminating Resistor of 50 Ω)

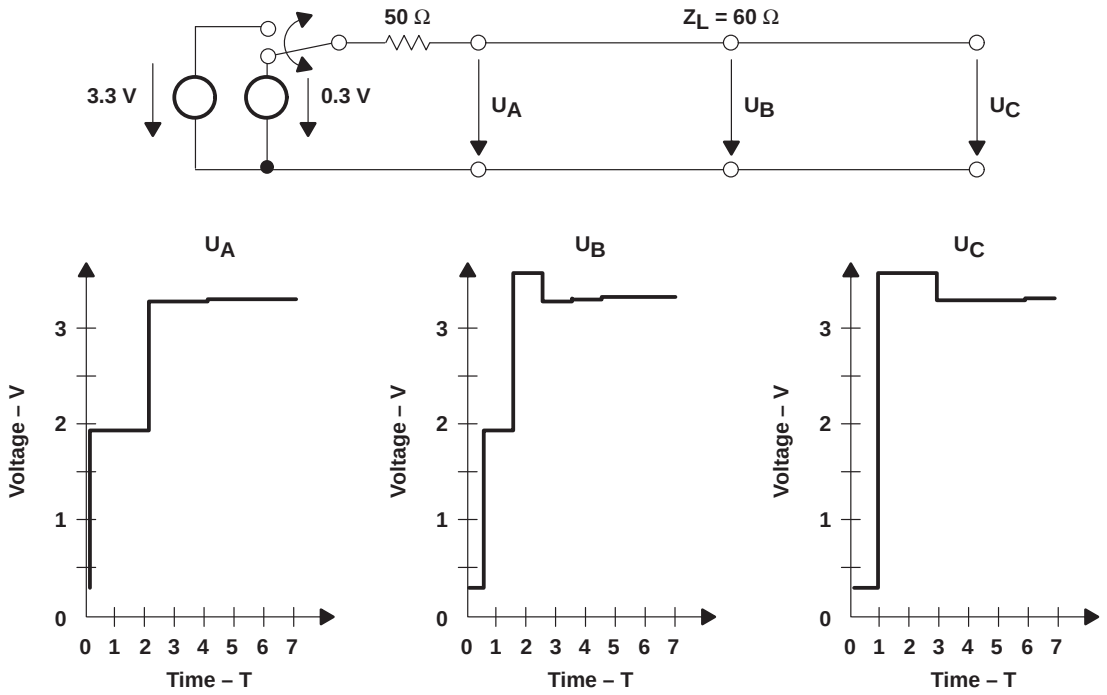


Figure 7. Voltage Waveforms With Incorrect Termination (Z_L = 60 Ω, No Terminating Resistor)

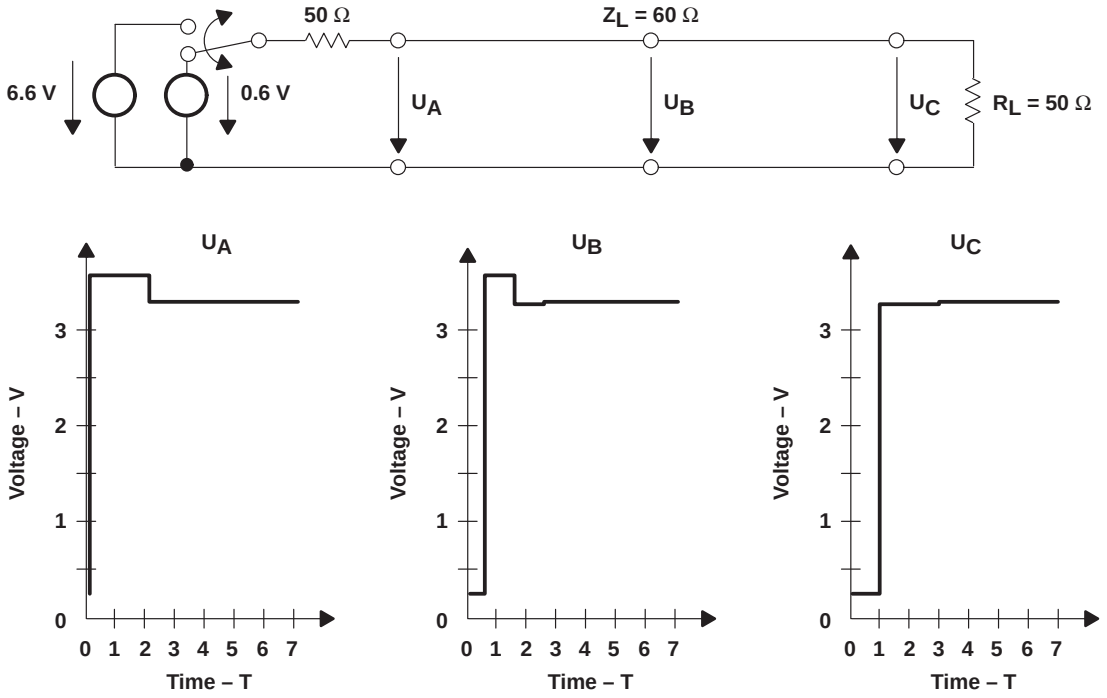


Figure 8. Voltage Waveforms With Incorrect Termination (Z_L = 60 Ω, Terminating Resistor of 50 Ω)

2.3 Impedance of Striplines

The characteristic dimension of a line is its impedance (Z_L), which, ignoring the resistive part, can be calculated as follows:

$$Z_L = \sqrt{\frac{L'}{C'}} \quad \textbf{(2)}$$

Where:

Z_L = impedance of the line
L' = inductance per unit of line length (nH/cm)
C' = capacitance per unit of line length (pF/cm)

The transit time (T) from the beginning to the end of the line can be calculated from the speed (v) of the signal:

$$v = \frac{1}{\sqrt{L' \times C'}} \quad \textbf{(3)}$$

$$T = \frac{l}{v} = l \times \sqrt{L' \times C'} \quad \textbf{(4)}$$

The two basic dimensions of a microstripline, the inductance per unit of line length (L') and the capacitance per unit of line length (C'), depend solely on the cross-sectional geometry and the relative permittivity (ε_r) (see Figure 9). The following expression can be deduced for the characteristic impedance of a microstripline:

$$Z_L = \frac{Z_O}{\sqrt{\epsilon_{r.eff}\frac{w_{eff}}{h}}} \quad \textbf{(5)}$$

Where:

Z_O = 120 π Ω; characteristic impedance of free space
$\varepsilon_{r.eff}$ = effective relative permittivity
w_{eff} = effective width of the microstripline
h = height of the dielectric

If $\varepsilon_r \leq 16$ and $w/h \geq 0.05$, the effective relative permittivity can be determined from equation 6 with a margin of error of < 1%.

$$\epsilon_{r.eff} = \frac{\epsilon_r + 1}{2} + \frac{(\epsilon_r - 1)F\left(\frac{w}{h}\right)}{2} \quad \textbf{(6)}$$

whereby the following applies:

if $w/h \leq 1$:

$$F\left(\frac{w}{h}\right) = \frac{1}{\sqrt{1 + 12\frac{w}{h}}} + 0.041\left(1 - \frac{w}{h}\right)^2$$

if $w/h \geq 1$:

$$F\left(\frac{w}{h}\right) = \frac{1}{\sqrt{1 + 12\frac{w}{h}}}$$

Where:

ε_r = relative permittivity of the dielectric
w = width of the microstripline
h = height of the dielectric

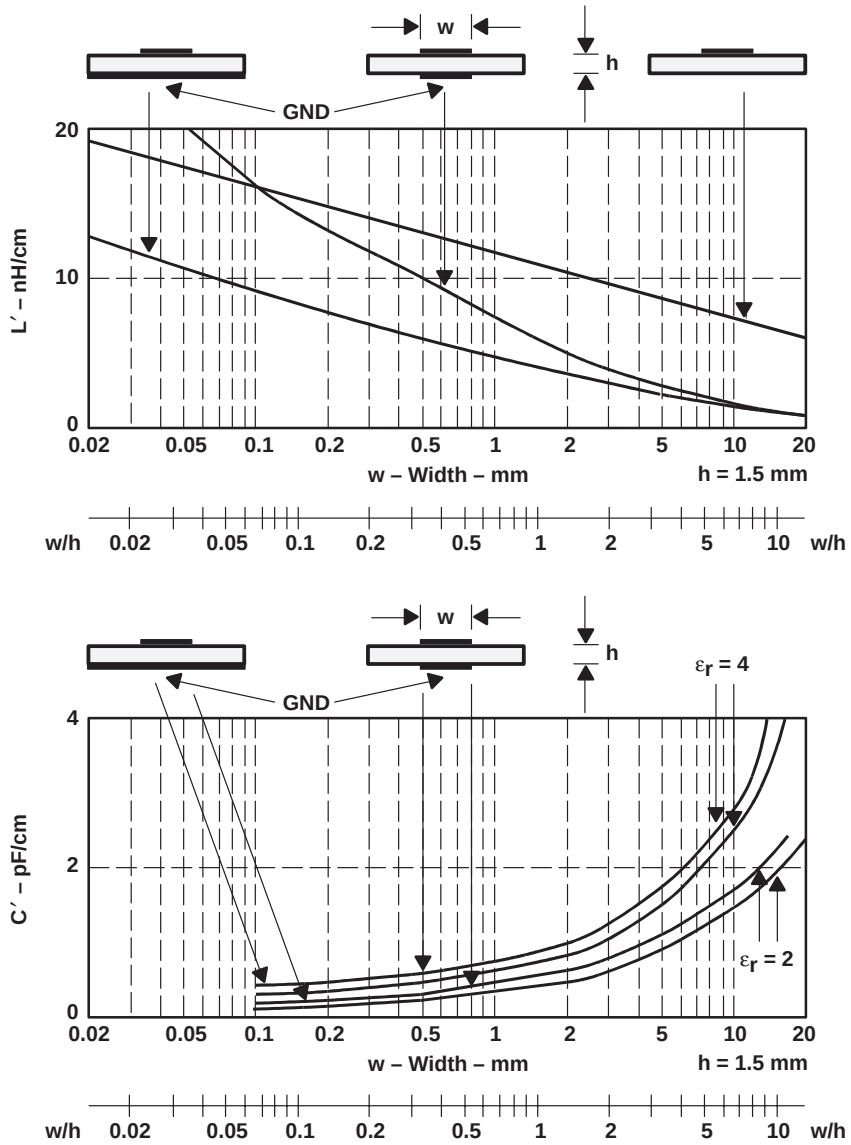


Figure 9. L′ and C′ of Microstriplines

The approximate ratio of the effective width of the microstripline to the width of the dielectric is determined using the following equation:

if w/h ≤ 1:

$$\frac{w_{eff}}{h} = 2\pi \frac{1}{\ln\left(8\frac{h}{w} + 0.25\frac{w}{h}\right)} \quad (7)$$

if w/h ≥ 1:

$$\frac{w_{eff}}{h} = \frac{w}{h} + 2.46 - 0.49\frac{h}{w} + \left(1 - \frac{h}{w}\right)^6$$

Where:

w = width of the microstripline
h = height of the dielectric

The characteristic impedance of a microstripline can be derived from the cross-sectional geometry and the relative permittivity of the circuit-board material using equations 5, 6, and 7. The curves in Figure 10, drawn using these calculations, show the characteristic impedance of a microstripline as a function of the parameters mentioned above.

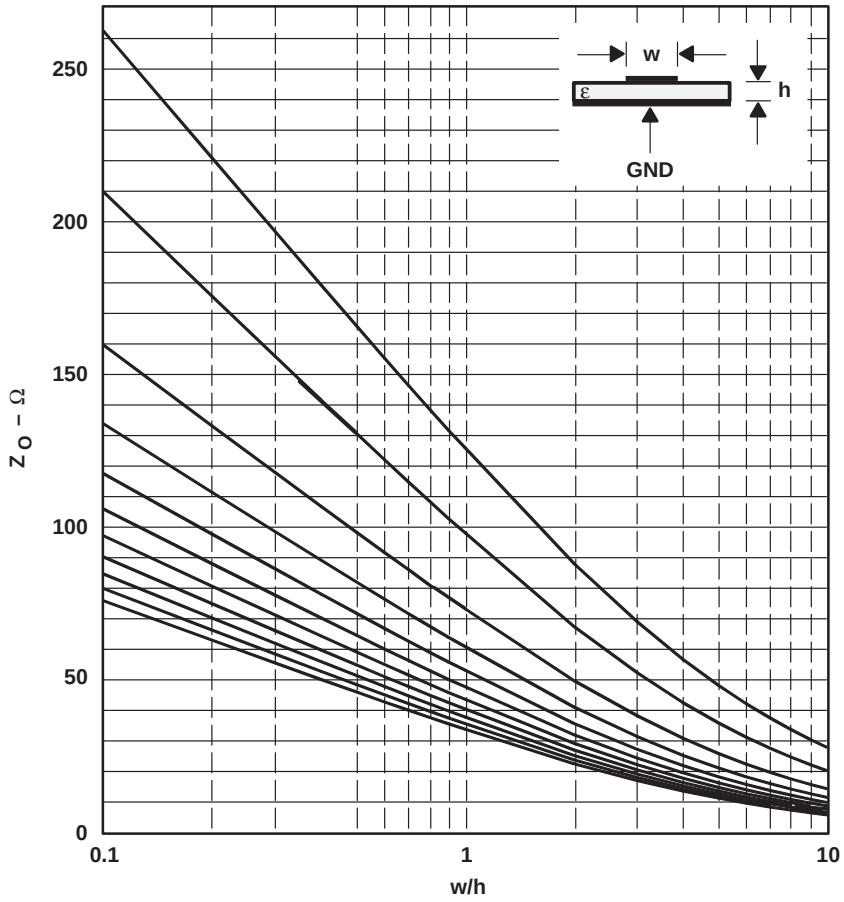


Figure 10. Characteristic Impedance of a Microstripline

Typical figures for the cross-sectional geometry and the dielectric constant for a line with a characteristic impedance of 50 Ω are given in Table 1.

Table 1. Typical Cross-Sectional Geometry and Dielectric Constant for a Line With a Characteristic Impedance of 50 Ω

w (μm)	h (μm)	ε_r	Z_L (Ω)
412	200	4.0	50.0
515	250	4.0	50.0
618	300	4.0	50.0
376	200	4.5	50.0
470	250	4.5	50.0
565	300	4.5	50.0
346	200	5.0	50.0
433	250	5.0	50.0
520	300	5.0	50.0

3 Test Setup

If the timing behavior of a fast logic circuit is evaluated, great care must be taken with the setup and the procedures used. Undistorted signals must be provided to the inputs of devices under test. Outputs must not be subjected to outside interference, apart from that of the intended capacitive and resistive loads. Bidirectional channels are particularly critical in this respect, because the direction in which the signal flows must be reversed during testing. In most cases, impedance matching is not possible, so bidirectional channels should be avoided for laboratory tests. For measurements in each direction, these channels should be configured as pure inputs or outputs.

3.1 Inputs

When evaluating timing behavior, the inputs of the device under test must have undistorted pulse edges. Generally, signal generators are provided with an output resistor of 50 Ω. In such cases, either series matching (see Figure 2a) or matching with a terminating resistor (see Figure 2b) can be used.

It is important that the input resistance of the device under test be considerably greater than the characteristic impedance. This is the case with currently available digital circuits and a 50-Ω line.

Series matching to the characteristic impedance is the usual method used with automatic testers. Although the signal waveform at the end of the line is undistorted, along the line there will be steps in the pulse edges. In such cases, if an oscilloscope is used, it should be connected directly at the input of the device under test.

In the laboratory, matching with a terminating resistor is the most commonly used method. The waveform of the signal along the line will not change, although the position, in time, of the signal pulse edge will vary with the signal delay time. The voltage level at the device under test will be half that at the signal source; signal generators currently available account for this.

A further important aspect when dimensioning lines is the differences of signal delay times. All lines must be the same length if all signals are to have the same delay times. If they are of different lengths, the positions of the pulse edges will no longer conform to those at the generator. The signal generator must be adjusted according to the length of the line.

3.2 Outputs

The outputs of the device under test are usually not provided with a defined output resistance. Often, there is a considerable difference between the output resistances at high and at low levels. For example, the SN74F245 is a digital IC with a bipolar output, whose output resistance changes from about 30 Ω at high level to between 3 Ω and 4 Ω at low level. In this case, line matching is difficult. Figure 11 shows the theoretically calculated waveforms at the beginning and end of a line of an unterminated 50-Ω line driven by an SN74F245. Usually, it is not necessary that the device being tested should drive a line.

Outputs usually have defined loads that should be as close as possible to the device under test.

An oscilloscope with a high resistance probe is usually used for precise measurement of timing behavior. Therefore, the input resistance of the measuring instrument can be ignored. However, the capacitive loading of the output by the probe may need to be taken into account.

All these requirements lead to the conclusion that, at the output:

- The load circuit and the probe head should be positioned as close as possible to the device under test.
- No stub line should be connected to the output (see Figure 11).

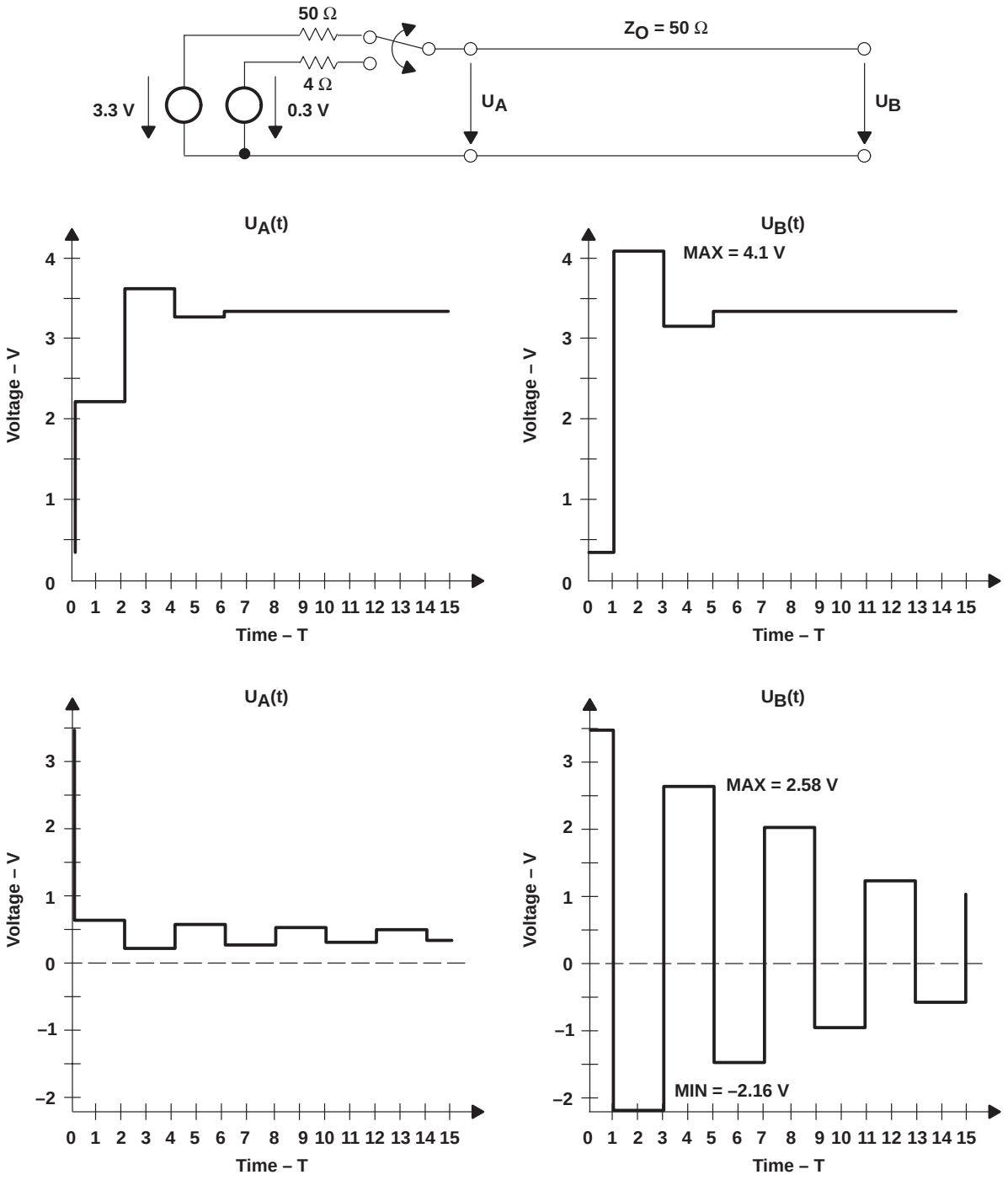


Figure 11. Theoretically Calculated Waveform at the Beginning and End of an Unterminated 50-Ω Line Driven by an SN74F245

Often, when evaluating the timing behavior of ICs, a load of 500 Ω and 50 pF to GND is specified. Figure 12 shows a measuring instrument with an input resistance of 50 Ω that solves the loading problem. The 50-Ω input resistance of the measuring instrument behaves as the terminating resistance of the 50-Ω line, although it is part of the 500-Ω load resistance. Thus, a 10:1 potential divider has been created, made up of the 450-Ω series resistor and the 50-Ω input resistance of the measuring equipment. When evaluating test results, the 10:1 potential divider and the signal transit time along the 50-Ω line to the test equipment must be taken into account. Again, the load capacitance of 50-pF should, if possible, be placed close to the output of the device under test.

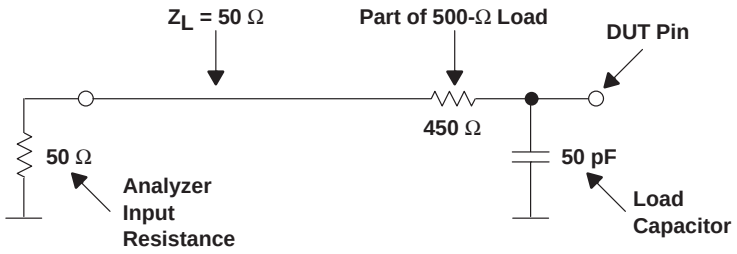


Figure 12. Decoupling of a Signal Using a Load of 500 Ω and 50 pF to GND and Test Equipment With an Input Resistance of 50 Ω

3.3 Bidirectional Connections

A line termination for both signal directions is seldom possible with bidirectional channels. If measurements are made at line terminations, each measurement should be connected as pure inputs or outputs.

3.4 Supply Voltage

The voltage supplying the device under test must show no changes, even with high-frequency current variations. This can be ensured by taking these precautions:

- There must be a low-resistance connection from the voltage source to the device under test. Preferably, each circuit board should have a separate layer for the supply voltage.
- The supply voltage must be decoupled by connecting a capacitor to the device under test. This capacitor must have very good characteristics at high frequencies, i.e., low inductance. Ceramic capacitors of about 100 nF are suitable for this purpose.

3.5 Example of a Test Setup

A test setup for laboratory evaluations has been developed by Texas Instruments to meet the following requirements:

- Connections from the signal generator to the input of the device under test must have a characteristic impedance of 50 Ω
- Connections from the generator to the input of the device must be the same length
- The load must be connected directly to the device under test
- No stub lines at outputs
- Low-resistance connections to the supply voltage
- A flexible layout, allowing the setup to be used for a variety of different measurements

To achieve this flexibility, the test circuitry was built on separate circuit boards:

1. ac-test motherboard
2. ac-test device-under-test (DUT) board for each type of measurement

Placing the circuitry on two boards allows a high degree of flexibility for the various measurements, with outstanding electrical performance at the lowest possible cost.

All signal connections to both circuit boards have a characteristic impedance of 50 Ω. As a result of the materials used and distances between layers resulting from the manufacturing process, the cross-sectional line geometries shown in Table 2 were achieved.

Table 2. Sectional Geometries of the Test-Setup Circuit Boards

w (μm)	h (μm)	ε_r	Z_L (Ω)
418	300	4.35	50.0

3.5.1 ac-Test Motherboard

The ac-test motherboard has five internal layers. One of each is used for the three voltage sources (DPS1, DPS2, and DPS3); the ground connection is made with two separate layers, and the layers are brought out with banana-plug sockets.

The board has HF sockets for a maximum of 84 channels that provide connections for word and pulse generators. These sockets are arranged in a circle to ensure the same line length from socket to test device. These sockets connect to an interconnection area through 50-Ω lines. This area has jumpers that allow the flexible configuration of each channel individually (see Figure 13). Signals that are applied to the device under test can be chosen as follows:

- Signal from the generator via the HF plug
- Supply voltage DPS1
- Supply voltage DPS2
- Supply voltage DPS3
- Ground connection

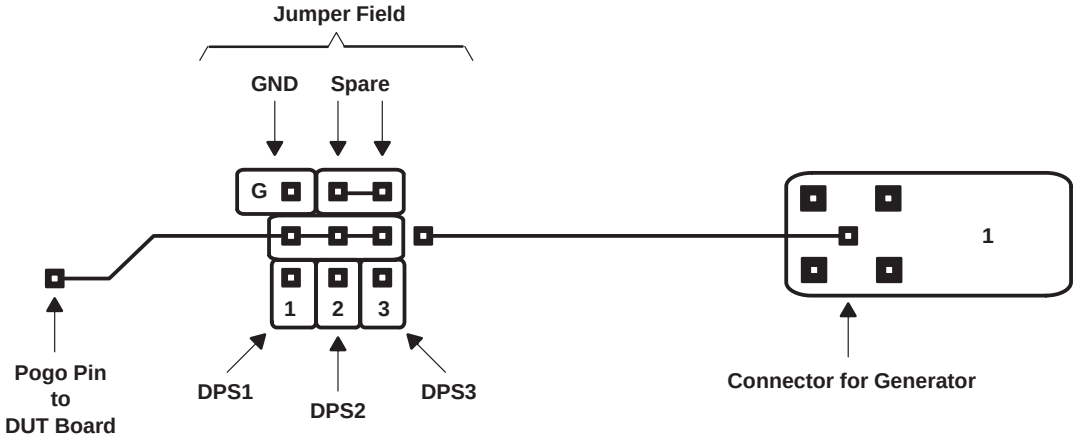


Figure 13. Interconnection Area for the Configuration of Each Channel

The signal goes from the interconnection area to the Pogo pins, arranged in a circle, which pass the signal on to the ac-test DUT board.

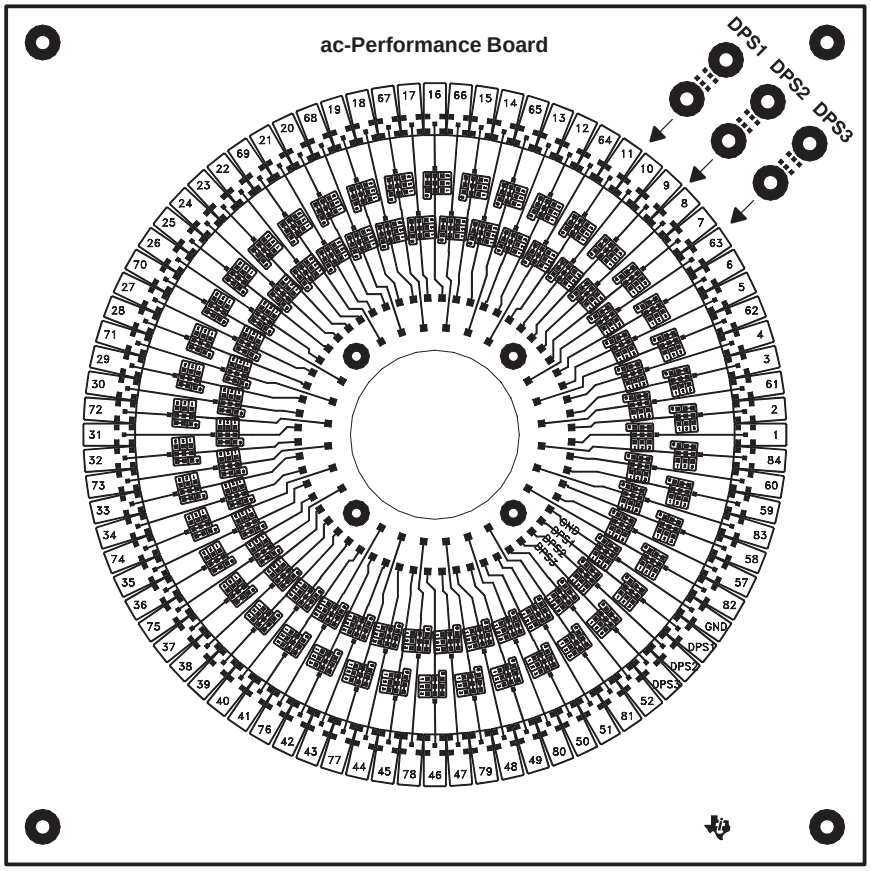


Figure 14. ac-Test Motherboard Rev. 2.0

3.5.2 ac-Test DUT Board

As an example of a DUT board, the circuit board for the SN74ACT7801FN 1024 × 18 first-in, first-out (FIFO) memory with a 68-pin plastic chip-carrier package is used. This IC has 27 inputs, 22 outputs, nine V_{CC} connections, and ten GND connections.

A track on the circuit board can be used equally well for either inputs or outputs.

The signal from the ac-test motherboard was taken to the input of the DUT using a jumper (a 0-Ω resistor). The circuit at the input of the DUT (see Figure 15) includes a 50-Ω terminating resistor between the end of the line and GND.

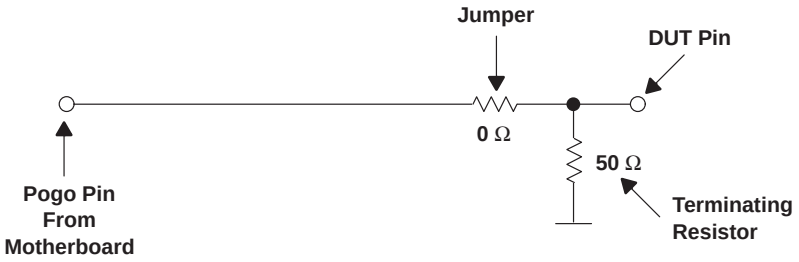


Figure 15. Circuit at the Input of the SN74ACT7801FN DUT Board

The jumper mentioned previously is removed when making timing measurements at the output pins. In this way, there are no unterminated stub lines at the output, and reflections are avoided. In addition, there is the possibility of soldering load circuits to V_{CC} and to GND (see Figure 16). The layout of the circuit board also allows the connection of measuring instruments with an input resistance of 50 Ω (see Figure 17).

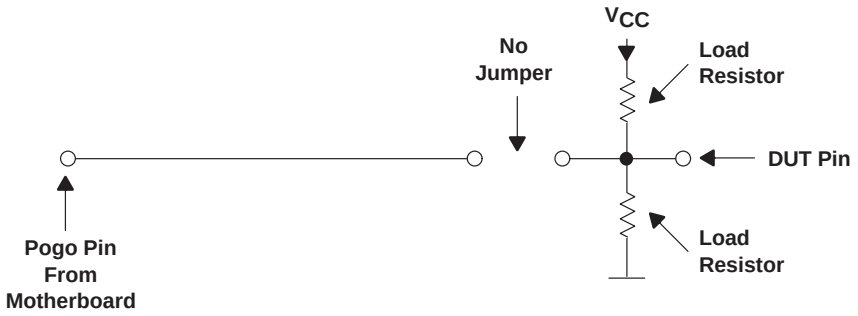


Figure 16. Circuit of an Output of the SN74ACT7801FN DUT Board

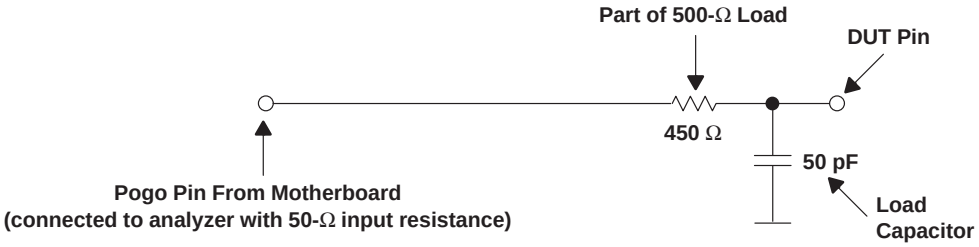


Figure 17. Circuit of an Output of the SN74ACT7801FN DUT Board With a Load Circuit of 500 Ω/50 pF to GND, Assuming a Signal Analyzer With an Input Resistance of 50 Ω

Jumpers, terminating resistors, and the load circuit are as close as possible to the DUT. These passive components are in space-saving surface-mount device (SMD) packages. The jumper is soldered to the topside of the board; the terminating resistor or the load circuit is on the underside (see Figure 18). The complete layout of the topside and underside of the DUT board for the SN74ACT7801FN is shown in Figures 19 and 20.

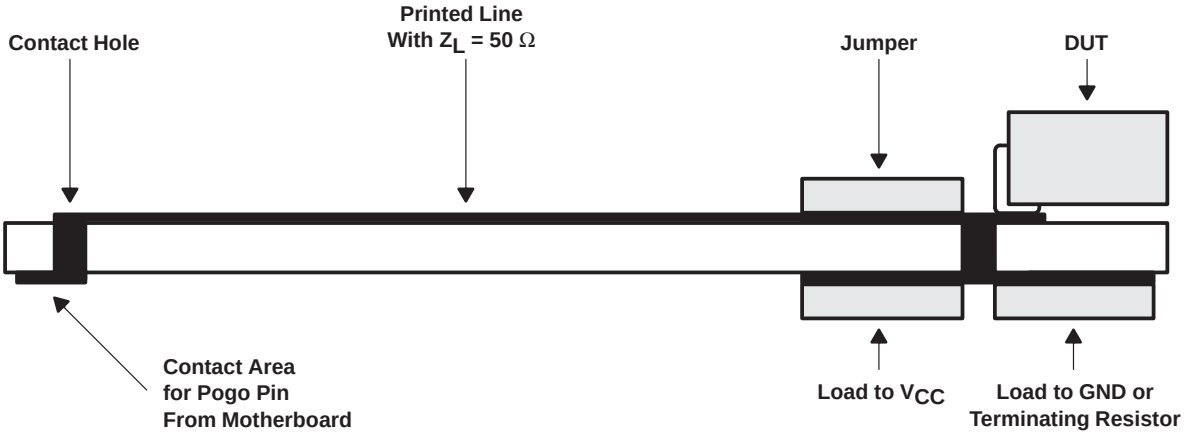


Figure 18. Cross-Section of the SN74ACT7801FN DUT Board, With the Printed Line and the Position of Passive Components for One Input or Output

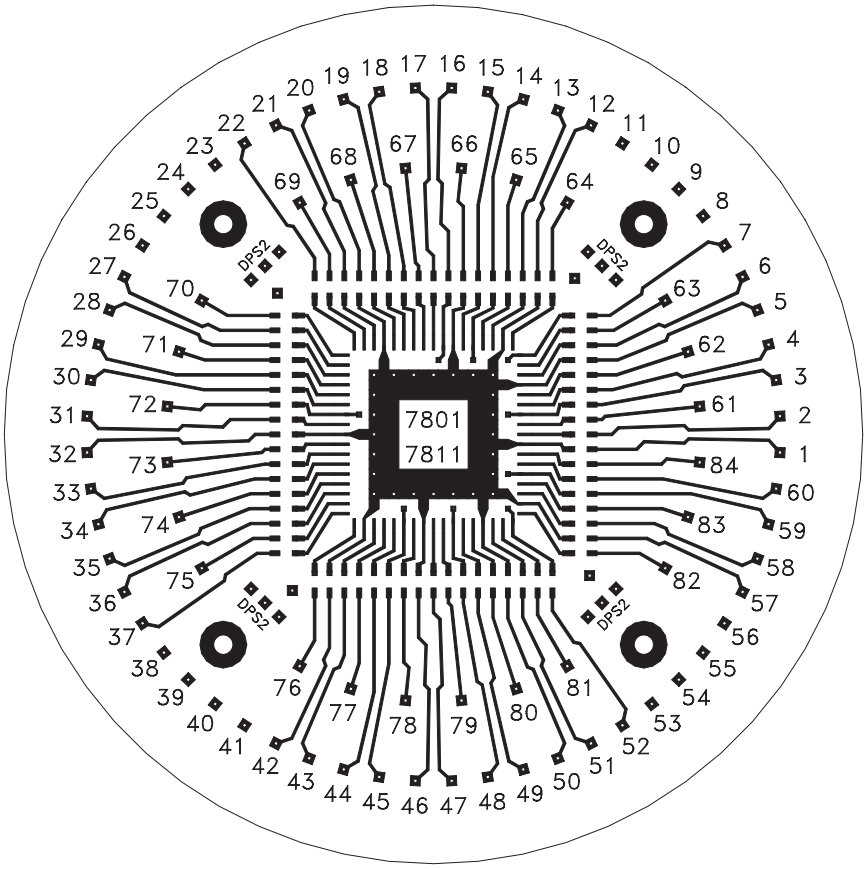


Figure 19. Topside of the ac-Test DUT Board for the FIFO SN74ACT7801FN in 68-Pin PLCC Package

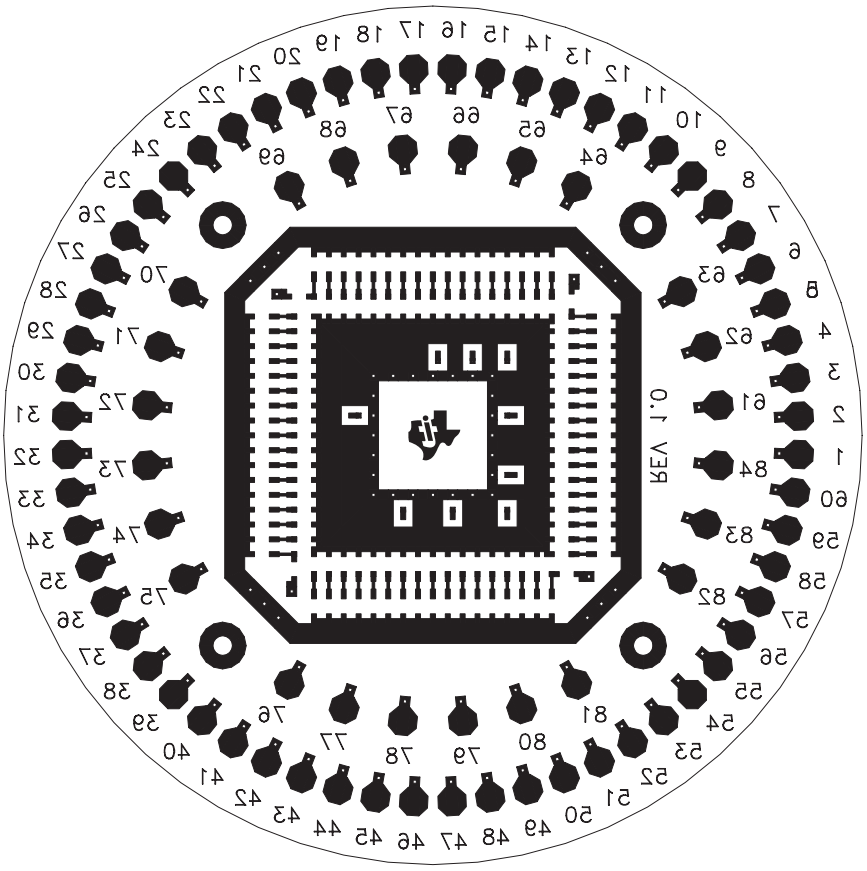


Figure 20. Underside of the ac-Test DUT Board for the FIFO SN74ACT7801FN in 68-Pin PLCC Package

3.5.3 Test Results With ac-Test Motherboard

The test setup described in the previous section has been fully evaluated. The ac-test motherboard Rev. 2.0 was used with the ac-test DUT board for the SN74ACT7801FN FIFO. The tests included all jumper connections, the Pogo pins, and the jumper field. The attenuation as a function of frequency was measured with the HP8505A Network Analyzer and HP8503 S-Parameter Test Set. Results of the measurements are shown in Figure 21. Only at 910 MHz was there an attenuation of 3 dB.

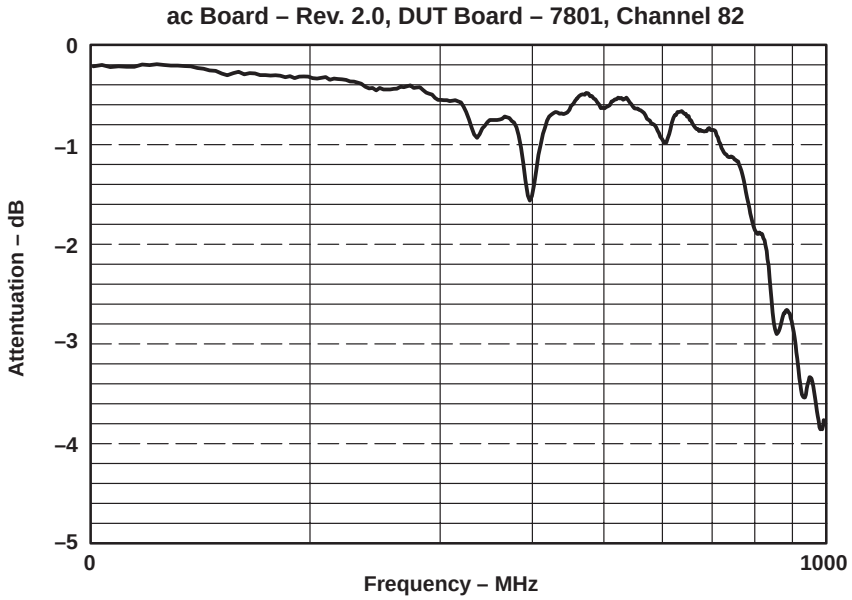


Figure 21. Transmission Loss Measured on Channel 82 of the ac-Test Motherboard Connected to the ac-Test DUT Board for the SN74ACT7801FN FIFO

Measurements with various DUT boards led, in some cases, to considerably lower limiting frequencies, which demonstrates that the DUT board must also be constructed with great care if precise measurement results are desired.

4 Summary

When evaluating the timing behavior of circuits that produce very steep pulse edges, an appropriate test setup is essential to achieve reliable, repeatable, and comparable test results. A good test setup has these characteristics:

- Each supply voltage and the ground connection should have separate layers on the circuit board. This ensures a stable voltage supply that will not change, even when there are high-frequency current fluctuations.
- The wiring on the test boards must have a defined characteristic impedance, normally 50 Ω, and be terminated with a series or a load resistor. This provides undistorted signals free from overshoot, undershoot, and without steps on the pulse edges to the input of the device under test.
- There must be no stub lines at the output, otherwise reflections will be generated. For this reason, the load circuit must be as close as possible to the device under test.
- Test equipment must be suitable for measurements to be made and its influence on the complete test setup recognized.

If these requirements are met, accurate and orderly measurements can be made.

Acknowledgment

The author of this document is Peter Forstner.

Appendix A

ac-Performance Board Documentation

A-1 Introduction

The construction, operation, and typical applications of the ac-performance board are presented in this appendix. The ac-performance board has the following features:

- The contacts of the device-under-test (DUT) are compatible with industrial-standard 84-pin DUT boards.
- It is possible to switch the input to up to 80 pins.
- Three separate dc-voltage connection options are available.
- Suitable for measuring characteristic curves
- Suitable for simultaneous-switching applications
- Suitable for all common ac measurements

A-2 Specifications

A-2.1 Mechanical Dimensions

Performance board

Length	300 mm
Width	300 mm
Thickness	3.0 mm

DUT board

Diameter	110 mm
Thickness	3.0 mm

A-2.2 Electrical Characteristics

Performance board

Capacitance between signal and ground level	300 mm
Impedance of signal line	300 mm
Difference of delay times between signal lines without DUT board	3.0 mm

DUT board

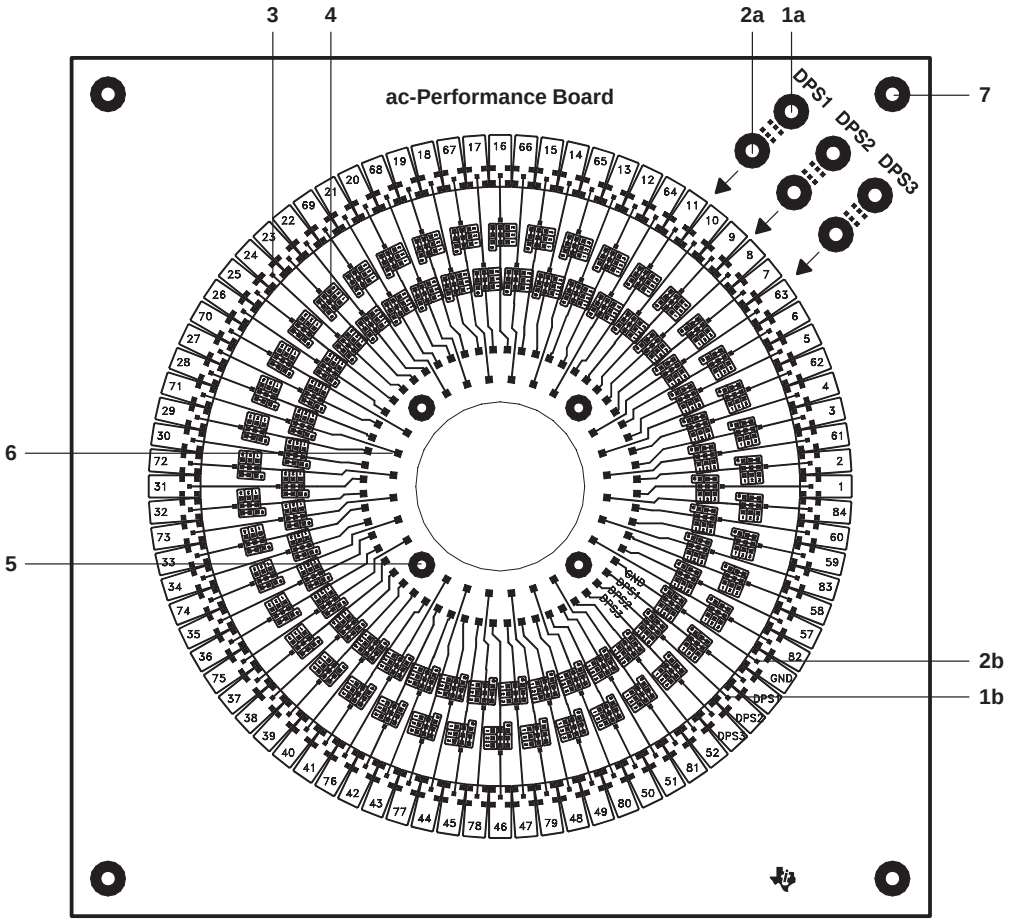
Impedance of signal line	300 mm

A-2.3 Temperature Range

Temperature range	–40°C to 110°C

A-3 Description of Operation

A-3.1 ac-Performance Board



1a, 1b	Separate dc-voltage connections (DPS1, DPS2, DPS3)
2a, 2b	Ground connection options (3)
3	Signal connectors (SMB)
4	Jumper matrix (detailed information in paragraph A-3.2)
5	Screw and grounding connection to the DUT board
6	Signal connections to DUT boards via Pogo pins
7	Holes for spacers (4)

Figure A-1. ac-Performance Board

A-3.2 Jumper Matrix

The jumper matrix allows connecting various dc voltages (DSP1, DSP2, DSP3) or GND, via gold bridges, to each signal pin. A connection between the SMB contact and the Pogo pin can be made with a gold bridge in the signal path.

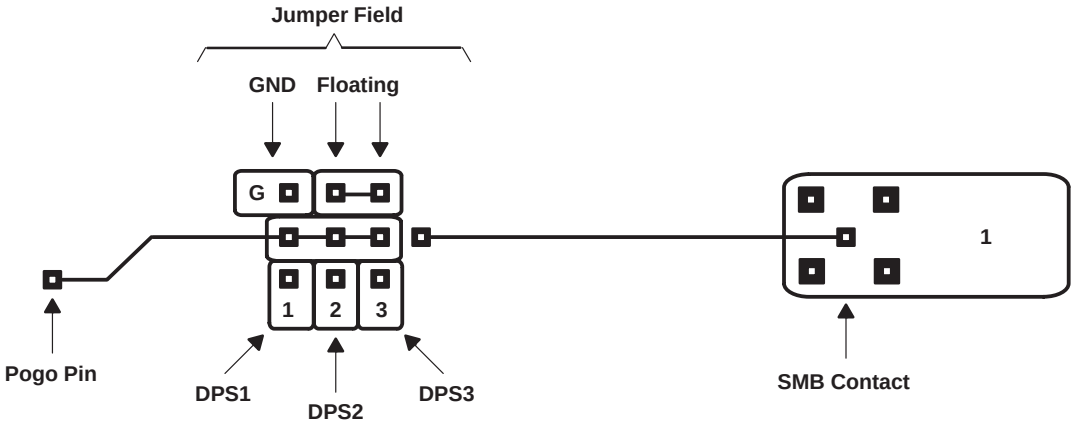
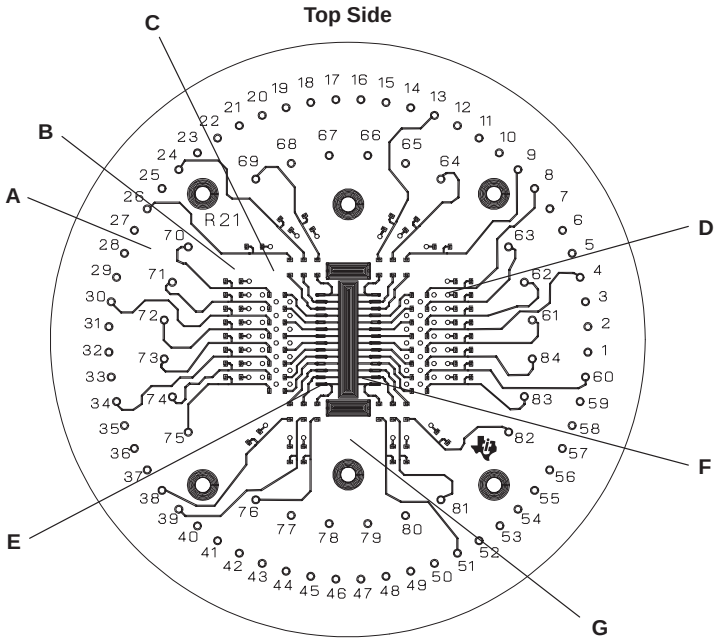
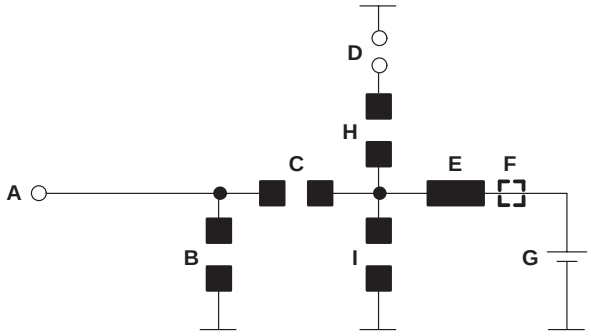


Figure A-2. Jumper Matrix

A-3.3 DUT Board Rev. 21 for 24-/28-Pin SO Package

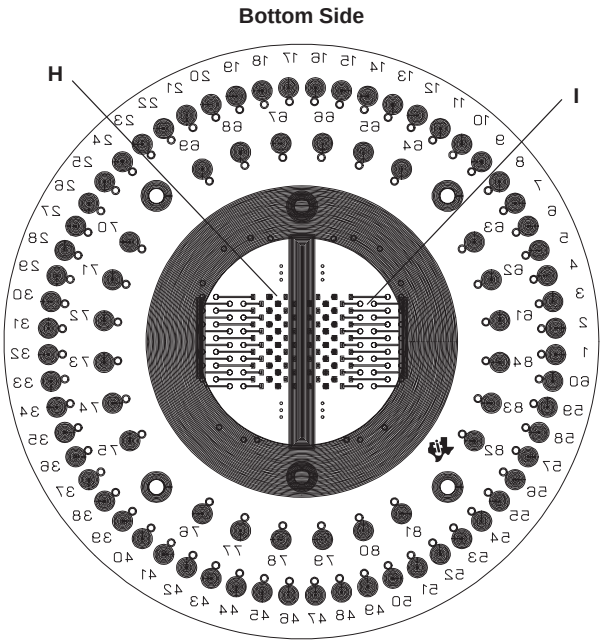


Layout of Each Channel



- **A** Connection to Pogo pin
- **B** SMD contact to ground and connection to Pogo pin 56
- **C** SMD contact for input bridges
- **D** Connection for 50-Ω cable
- **E** IC pin contact area
- **F** Optional point to isolate the IC from V_{CC}
- **G** V_{CC} connection to Pogo pin 56
- **H** SMD contact for series resistor from the connector for 50-Ω cable
- **I** SMD contact to ground and connection to Pogo pin 56

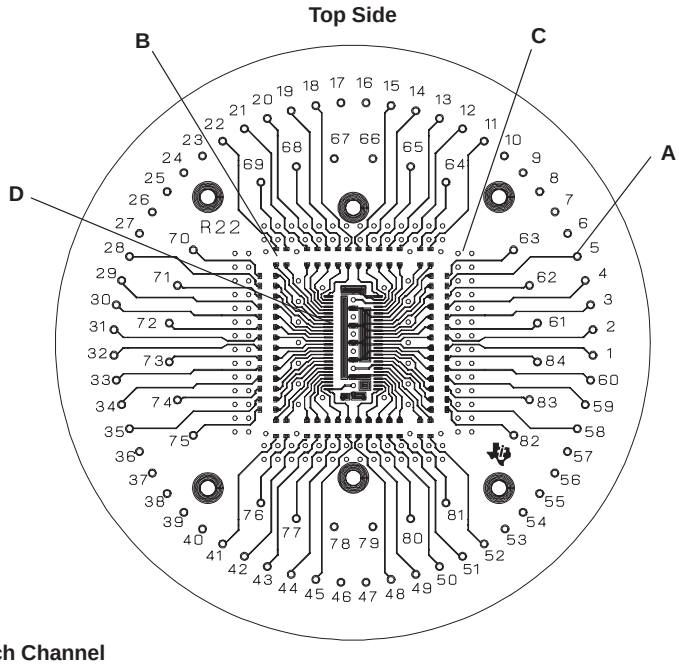
Figure A-3. DUT Board Rev. 21 (Top)



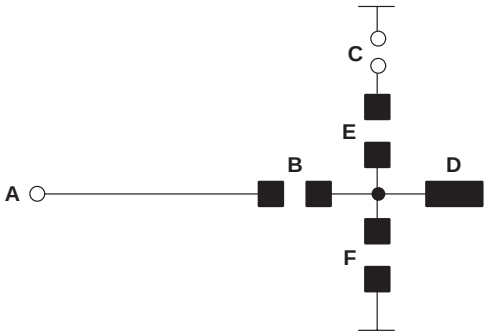
H SMD contact for series resistor from the connector for 50-Ω cable
I SMD contact to ground and connection to Pogo pin 56

Figure A-4. DUT Board Rev. 21 (Bottom)

A-3.4 DUT Board Rev. 22 for 56-Pin SSO Package

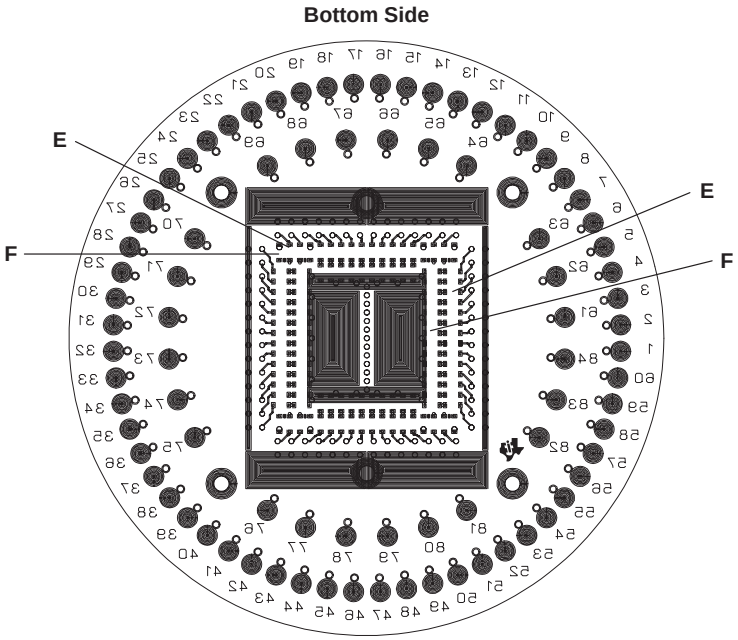


Layout of Each Channel



A Connection to Pogo pin
B SMD contact for input bridge
C Connection for 50-Ω cable
D IC pin contact area
E SMD contact for series resistor from the connector for 50-Ω cable
F SMD contact to ground and connection to Pogo pin 56

Figure A-5. DUT Board Rev. 22 (Top)



E SMD contact for series resistor from the connector for 50-Ω cable
F SMD contact to ground and connection to Pogo pin 56

Figure A-6. DUT Board Rev. 22 (Bottom)

A-3.5 DUT Board Rev. 23 for 100-Pin SQF Package

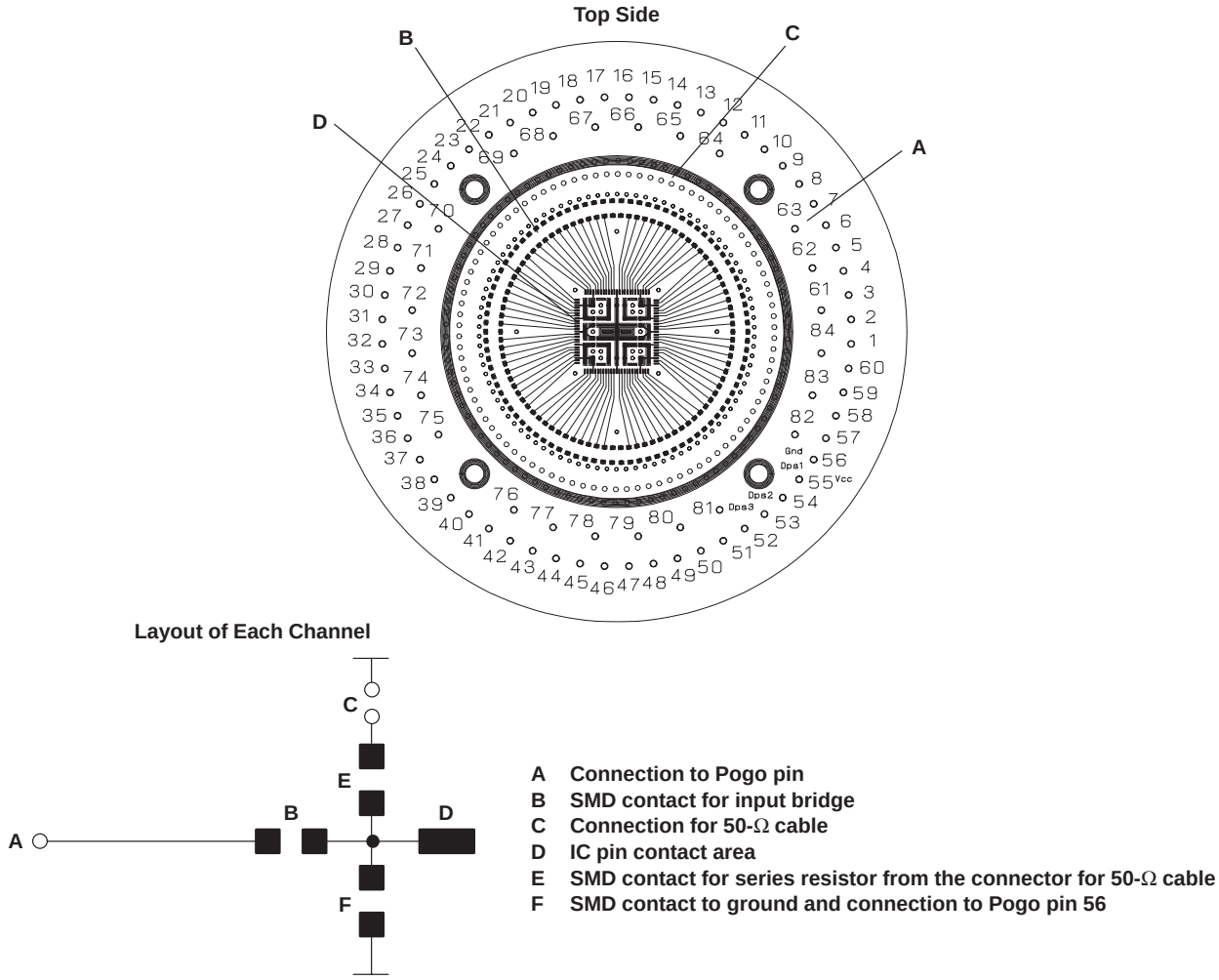
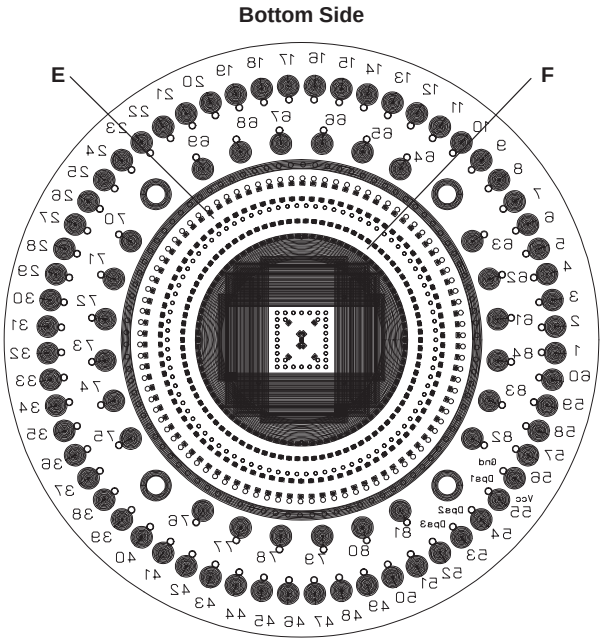


Figure A-7. DUT Board Rev. 23 (Top)



E **SMD contact for series resistor from the connector for 50-Ω cable**
F **SMD contact to ground and connection to Pogo pin 56**

Figure A-8. DUT Board Rev. 23 (Bottom)

A-4 Description of Applications

A-4.1 Measuring Transit Time

The oscilloscope inputs have an impedance of 50 Ω. The effective load capacitance includes the specific load capacitance at the output plus the board capacitance.

All connections from generator to board, generator to oscilloscope, and oscilloscope to board are made with 50-Ω cable.

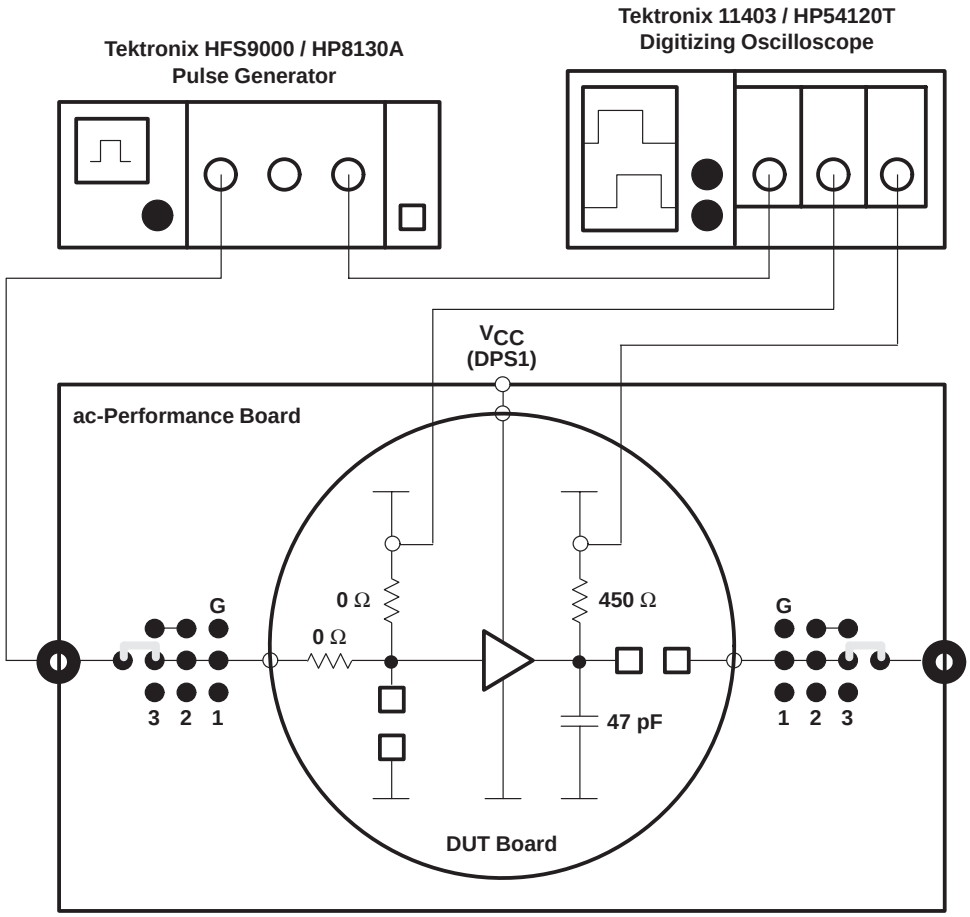


Figure A-9. Transit-Time Measurement Setup

A-5 Description of Signals

A-5.1 Signal Waveforms

The curves in Figure A-10 have been measured with the test setup described in paragraph A-4.1 Measuring Transit Time.

The device under test is a ABT32501, soldered on the DUT board Rev. 23. The ABT32501 has been configured to measure the propagation delay time (t_{PHL}/t_{PLH}) of one driver (1A1 to 1B1).

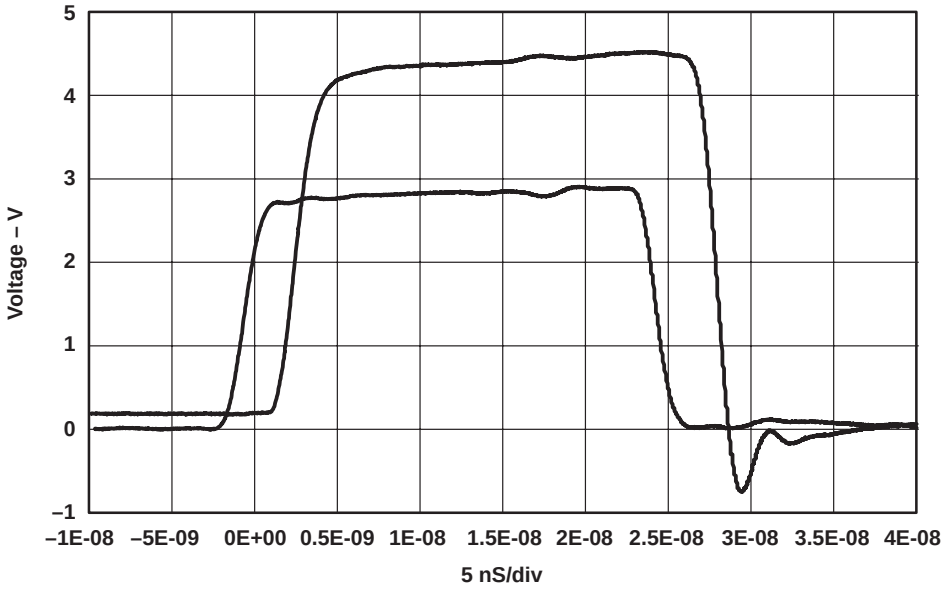


Figure A-10. Signal Waveforms Using ac-Performance Board and DUT Board Rev. 23

A-5.2 Description of the Transmission-Loss Measurement

Measured values were determined using the HP8505A Network Analyzer and the HP8503 S-Parameter Test Set (see Figure A-11). As the test setup shows, the measurement has been made using one channel of the ac-performance board in conjunction with the DUT board Rev. 23 and a combination of two channels. Here it was important to include the complete lines of the DUT board of each channel.

Results of the transmission-loss measurement are shown graphically in paragraph A-5.3.

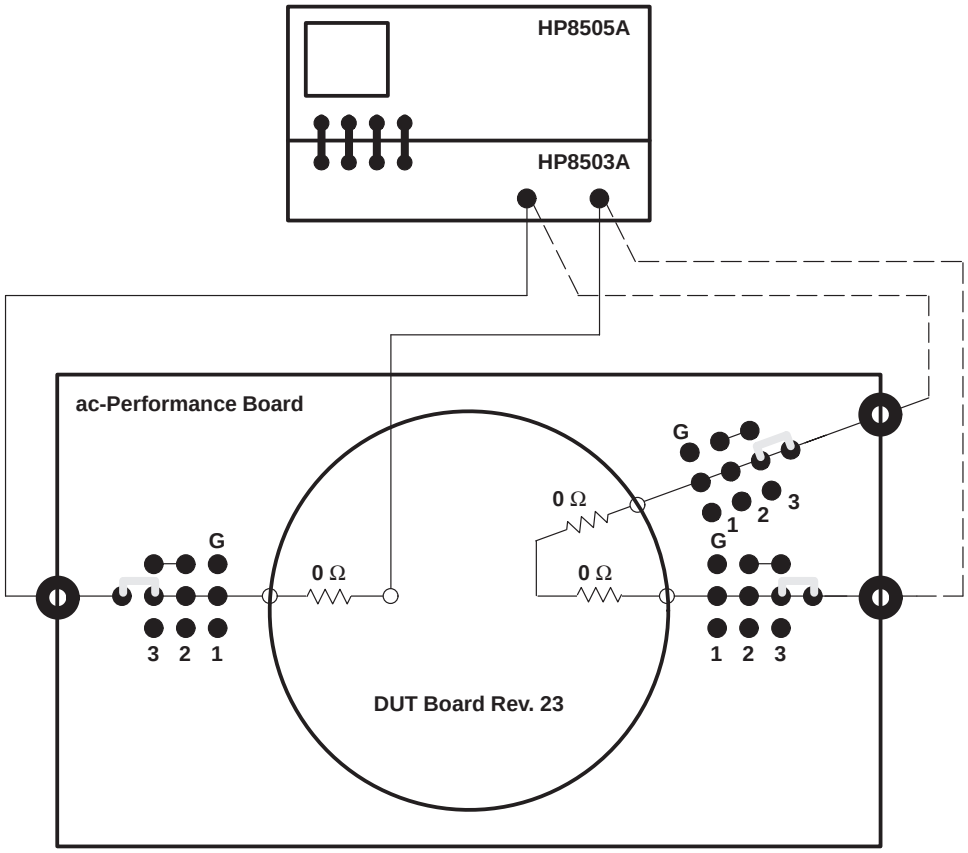


Figure A-11. Principal Test Setup for Transmission-Loss Measurement

A-5.3 Results of the Transmission-Loss Measurement

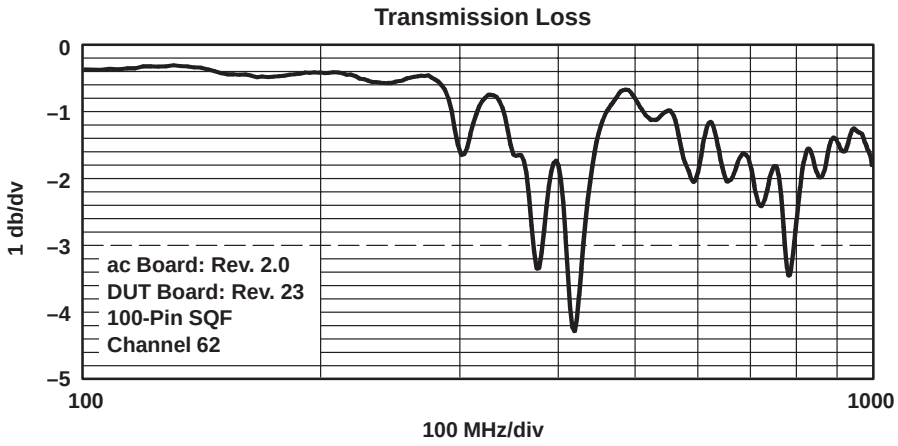


Figure A-12. Frequency Dependency of the Transmission Loss Using Channel 62 of the ac-Performance Board in Conjunction With the DUT Board Rev. 23

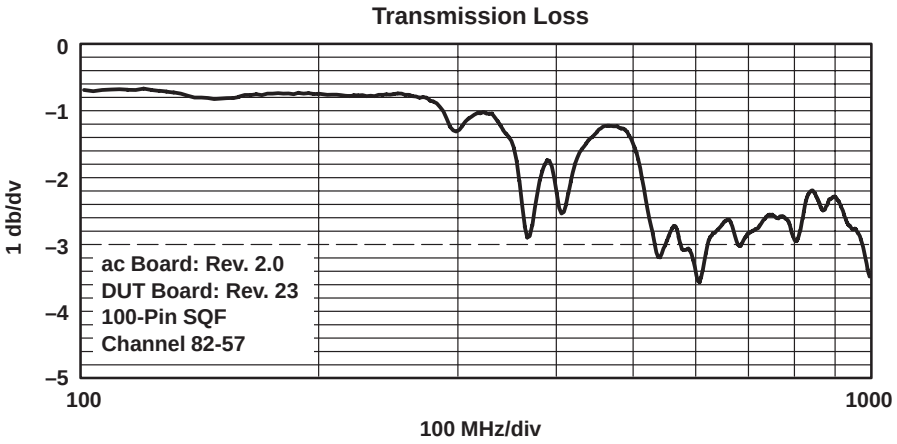


Figure A-13. Frequency Dependency of the Transmission Loss Using Channel 82-57 of the ac-Performance Board in Conjunction With the DUT Board Rev. 23

A-5.4 Description of the TDR Measurement

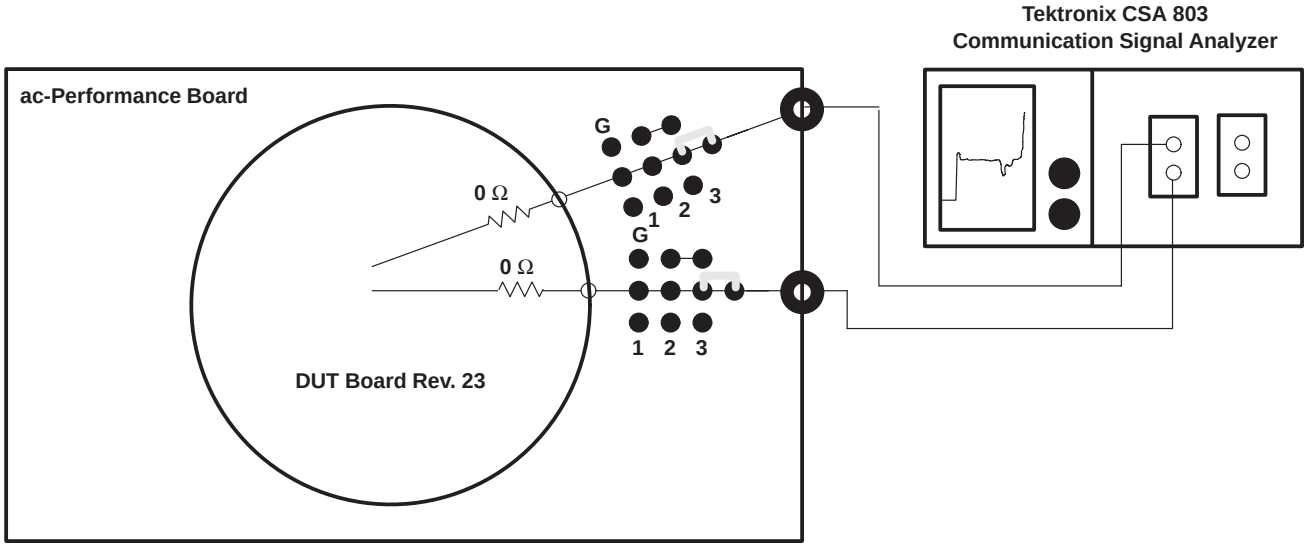


Figure A-14. Principal Test Setup for the TDR Measurement

The measurement was made using a Tektronix CSA 803 Communication Signal Analyzer with a special Sampling Head (SD-24, 20 GHz). To make this measurement, a voltage slope with defined amplitude must be applied to the test line. Analyzing the waveform at the signal source leads to the impedance and the delay time of the line. The CSA 803 makes the calculation and shows the impedance and the delay time directly. A signal generator with a defined resistance (R_i = 50 Ω) is integrated in the sampling head. It generates an amplitude of U = 500 mV with a rise time of about 25 ps. A second internal generator is available in the sampling head.

Because both generators can be driven in push-pull, the basic line dimension (Z_{Lodd}) of two symmetrical cross-coupled lines can be determined.

Paragraph A-5.5 shows, in the first figure, the time dependency of rho (ρ) for a single line. The result of two symmetrical cross-coupled lines is shown in the second figure.

The formula for the calculation of the impedance is:

$$Z_L = Z_O \frac{1 + \rho}{1 - \rho} \quad (1)$$

A-5.5 Result of the TDR Measurement

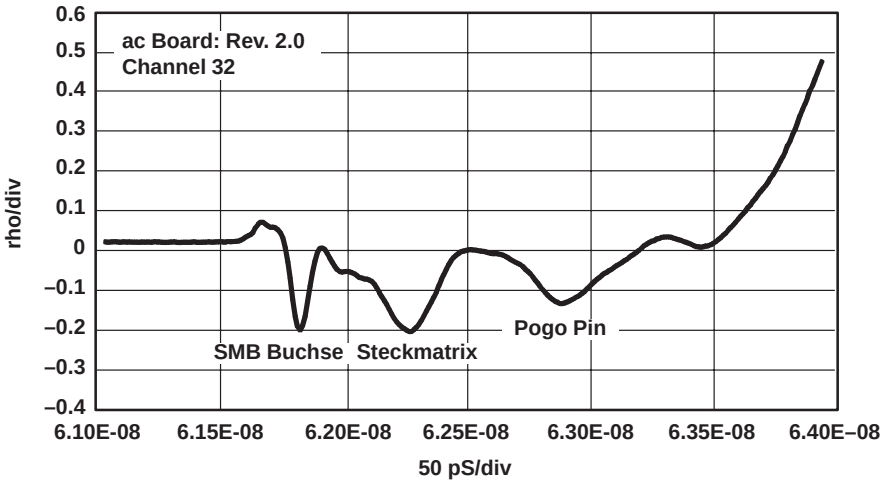


Figure A-15. Time Dependency of rho Using Channel 32 on the ac-Performance Board With the DUT Board Rev. 23

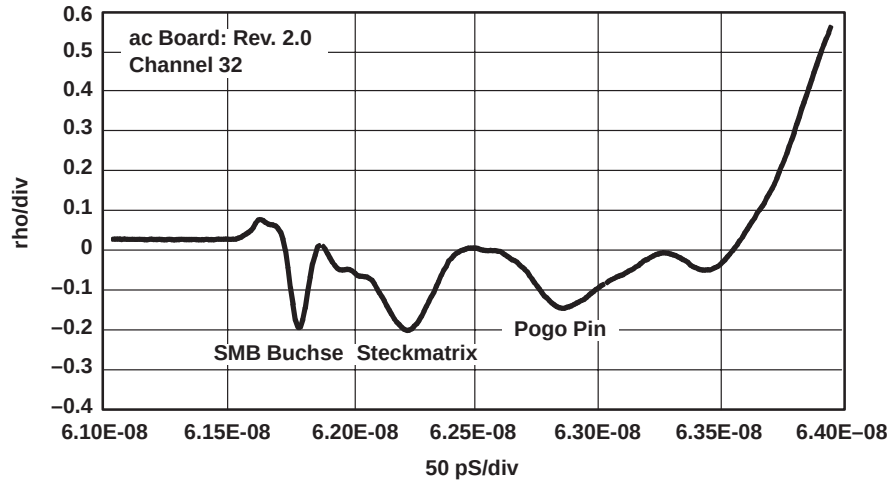


Figure A-16. Time Dependency of rho Using Channel 32 With the Symmetrical Cross-Coupled Channel 73 (in Push-Pull) on the ac-Performance Board With the DUT Board Rev. 23

A-6 Parts List

DESCRIPTION	SUPPLIER	PART NUMBER	QUANTITY
ac Board Rev. 2.0	Texas Instruments	AC-Board 2.0	1
Inset nuts ∅4.5	Bürklin	16H600	4
Sockets, black	Bürklin	25F220	3
Sockets, red	Bürklin	25F230	3
Hex posts M5	Bürklin	18H236	4
Hex nuts M5	Bürklin	16H7906	4
Washers ∅5.3	Bürklin	16H864	8
SMB plug	Bürklin	77F210	84
SMC plug	Suhner	82SMC-50-0-1	84
Sub mini sockets ∅1.0	Infratron	H3153-05	756
Pogo pins	Feinmetall	FM670/15	84
Sleeves	Feinmetall	FM6010-10 S003	84

Addresses of suppliers:

Hans Bürklin
Schillerstr. 40
D–80336 München

Feinmetall
Zeppelinstr. 2
D–71083 Herrenberg

Infratron
Am Schnepfenweg 34
D–80995 München

Suhner Elektronik GmbH
Mehlbeerenstr. 6
D–82024 Taufkirchen

Acknowledgment

The author of this appendix is Claus Kuch.