

## Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These designations are based on the more detailed timing information used by the development system and reported in the output files. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on characterization. Further changes are not expected.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. All specifications are subject to change without notice.

## DC Specifications

### Absolute Maximum Ratings<sup>(1)</sup>

| Symbol      | Description                                      | Min  | Max  | Units |
|-------------|--|------|------|-------|
| $V_{CCINT}$ | Supply voltage relative to GND                   | -0.5 | 2.0  | V     |
| $V_{CCO}$   | Supply voltage relative to GND                   | -0.5 | 4.0  | V     |
| $V_{REF}$   | Input reference voltage                          | -0.5 | 4.0  | V     |
| $V_{IN}$    | Input voltage relative to GND <sup>(2,3)</sup>   | -0.5 | 4.0  | V     |
| $V_{TS}$    | Voltage applied to 3-state output <sup>(3)</sup> | -0.5 | 4.0  | V     |
| $T_{STG}$   | Storage temperature (ambient)                    | -65  | +150 | °C    |
| $T_J$       | Junction temperature                             | -    | +125 | °C    |

#### Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- $V_{IN}$  should not exceed  $V_{CCO}$  by more than 3.6V over extended periods of time (e.g., longer than a day).
- Maximum DC overshoot must be limited to either  $V_{CCO} + 0.5V$  or 10 mA, and undershoot must be limited to -0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to -2.0V or overshoot to  $V_{CCO} + 2.0V$ , provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Packaging Information on the Xilinx website.

## Recommended Operating Conditions

| Symbol      | Description                                   |            | Min      | Max      | Units |
|-------------|---|------------|----------|----------|-------|
| $T_J$       | Junction temperature                          | Commercial | 0        | 85       | °C    |
|             |   | Industrial | -40      | 100      | °C    |
| $V_{CCINT}$ | Supply voltage relative to GND <sup>(1)</sup> | Commercial | 1.8 – 5% | 1.8 + 5% | V     |
|             |   | Industrial | 1.8 – 5% | 1.8 + 5% | V     |
| $V_{CCO}$   | Supply voltage relative to GND <sup>(2)</sup> | Commercial | 1.2      | 3.6      | V     |
|             |   | Industrial | 1.2      | 3.6      | V     |
| $T_{IN}$    | Input signal transition time <sup>(3)</sup>   |            | -        | 250      | ns    |

### Notes:

- Functional operation is guaranteed down to a minimum  $V_{CCINT}$  of 1.62V (Nominal  $V_{CCINT}$  -10%). For every 50 mV reduction in  $V_{CCINT}$  below 1.71V (nominal  $V_{CCINT}$  -5%), all delay parameters increase by 3%.
- Minimum and maximum values for  $V_{CCO}$  vary according to the I/O standard selected.
- Input and output measurement threshold is ~50% of  $V_{CCO}$ .

## DC Characteristics Over Operating Conditions

| Symbol       | Description   |                         | Min        | Typ | Max  | Units |    |
|--------------|---|-------------------------|------------|-----|------|-------|----|
| $V_{DRINT}$  | Data retention $V_{CCINT}$ voltage (below which configuration data may be lost)               |                         | 1.5        | -   | -    | V     |    |
| $V_{DRIO}$   | Data retention $V_{CCO}$ voltage (below which configuration data may be lost)                 |                         | 1.2        | -   | -    | V     |    |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current <sup>(1)</sup>   | XC2S50E                 | Commercial | -   | -    | 200   | mA |
|              |   |                         | Industrial | -   | -    | 200   | mA |
|              |   | XC2S100E                | Commercial | -   | -    | 200   | mA |
|              |   |                         | Industrial | -   | -    | 200   | mA |
|              |   | XC2S150E                | Commercial | -   | -    | 300   | mA |
|              |   |                         | Industrial | -   | -    | 300   | mA |
|              |   | XC2S200E                | Commercial | -   | -    | 300   | mA |
|              |   |                         | Industrial | -   | -    | 300   | mA |
|              |   | XC2S300E                | Commercial | -   | -    | 300   | mA |
|              |   |                         | Industrial | -   | -    | 300   | mA |
|              |   | XC2S400E                | Commercial | -   | -    | 300   | mA |
|              |   |                         | Industrial | -   | -    | 300   | mA |
| XC2S600E     | Commercial  | -                       | -          | 400 | mA   |       |    |
|              | Industrial  | -                       | -          | 400 | mA   |       |    |
| $I_{CCOQ}$   | Quiescent $V_{CCO}$ supply current <sup>(1)</sup>   |                         | -          | -   | 2    | mA    |    |
| $I_{REF}$    | $V_{REF}$ current per $V_{REF}$ pin   |                         | -          | -   | 20   | μA    |    |
| $I_L$        | Input or output leakage current <sup>(2)</sup>  |                         | -10        | -   | +10  | μA    |    |
| $C_{IN}$     | Input capacitance (sample tested)   | TQ, PQ, FG, FT packages | -          | -   | 8    | pF    |    |
| $I_{RPU}$    | Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 3.3V$ (sample tested) <sup>(3)</sup> |                         | -          | -   | 0.25 | mA    |    |
| $I_{RPD}$    | Pad pull-down (when selected) @ $V_{IN} = 3.6V$ (sample tested) <sup>(3)</sup>                |                         | -          | -   | 0.25 | mA    |    |

### Notes:

- With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
- The I/O leakage current specification applies only when the  $V_{CCINT}$  and  $V_{CCO}$  supply voltages have reached their respective minimum Recommended Operating Conditions.
- Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

## Power-On Requirements

Spartan-IIe FPGAs require that a minimum supply current  $I_{CCPO}$  be provided to the  $V_{CCINT}$  lines for a successful power-on. If more current is available, the FPGA can consume more than  $I_{CCPO}$  min., though this cannot adversely affect reliability.

A maximum limit for  $I_{CCPO}$  is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of  $I_{CCPO}$  by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

| Symbol     | Description   |            | Min <sup>(1)</sup> | Max | Units |
|------------|---|------------|--------------------|-----|-------|
| $I_{CCPO}$ | Total $V_{CCINT}$ supply current required during power-on | Commercial | 500                | -   | mA    |
|            |   | Industrial | 2                  | -   | A     |
| $T_{CCPO}$ | $V_{CCINT}$ <sup>(2,3)</sup> ramp time                    |            | 2                  | 50  | ms    |

### Notes:

- The  $I_{CCPO}$  requirement applies for a brief time (commonly only a few milliseconds) when  $V_{CCINT}$  ramps from 0 to 1.8V.
- The ramp time is measured from GND to 1.8V on a fully loaded board.
- $V_{CCINT}$  must not dip in the negative direction during power on.
- Power-on current is measured with  $V_{CCINT}$  and  $V_{CCO}$  powering up simultaneously.
- I/Os are not guaranteed to be disabled until  $V_{CCINT}$  is applied.
- For more information on designing to meet the power-on specifications, refer to the application note [XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIe Families"](#).

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $V_{OL}$  and  $V_{OH}$  are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all

standards meet their specifications. The selected standards are tested at minimum  $V_{CCO}$  with the respective  $I_{OL}$  and  $I_{OH}$  currents shown. Other standards are sample tested.

| Input/Output Standard | $V_{IL}$ |                  | $V_{IH}$         |                 | $V_{OL}$         | $V_{OH}$         | $I_{OL}$ | $I_{OH}$ |
|-----------------------|----------|------------------|------------------|-----------------|------------------|------------------|----------|----------|
|                       | V, Min   | V, Max           | V, Min           | V, Max          | V, Max           | V, Min           | mA       | mA       |
| LVTTL <sup>(1)</sup>  | -0.5     | 0.8              | 2.0              | 3.6             | 0.4              | 2.4              | 24       | -24      |
| LVCOS2                | -0.5     | 0.7              | 1.7              | 2.7             | 0.4              | 1.9              | 12       | -12      |
| LVCOS18               | -0.5     | 35% $V_{CCO}$    | 65% $V_{CCO}$    | 1.95            | 0.4              | $V_{CCO} - 0.4$  | 8        | -8       |
| PCI, 3.3V             | -0.5     | 30% $V_{CCO}$    | 50% $V_{CCO}$    | $V_{CCO} + 0.5$ | 10% $V_{CCO}$    | 90% $V_{CCO}$    | Note (2) | Note (2) |
| GTL                   | -0.5     | $V_{REF} - 0.05$ | $V_{REF} + 0.05$ | 3.6             | 0.4              | -                | 40       | -        |
| GTL+                  | -0.5     | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | 3.6             | 0.6              | -                | 36       | -        |
| HSTL I                | -0.5     | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | 3.6             | 0.4              | $V_{CCO} - 0.4$  | 8        | -8       |
| HSTL III              | -0.5     | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | 3.6             | 0.4              | $V_{CCO} - 0.4$  | 24       | -8       |
| HSTL IV               | -0.5     | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | 3.6             | 0.4              | $V_{CCO} - 0.4$  | 48       | -8       |
| SSTL3 I               | -0.5     | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 3.6             | $V_{REF} - 0.6$  | $V_{REF} + 0.6$  | 8        | -8       |
| SSTL3 II              | -0.5     | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 3.6             | $V_{REF} - 0.8$  | $V_{REF} + 0.8$  | 16       | -16      |
| SSTL2 I               | -0.5     | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 3.6             | $V_{REF} - 0.61$ | $V_{REF} + 0.61$ | 7.6      | -7.6     |
| SSTL2 II              | -0.5     | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 3.6             | $V_{REF} - 0.8$  | $V_{REF} + 0.8$  | 15.2     | -15.2    |
| CTT                   | -0.5     | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 3.6             | $V_{REF} - 0.4$  | $V_{REF} + 0.4$  | 8        | -8       |
| AGP                   | -0.5     | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 3.6             | 10% $V_{CCO}$    | 90% $V_{CCO}$    | Note (2) | Note (2) |

### Notes:

- $V_{OL}$  and  $V_{OH}$  for lower drive currents are sample tested.
- Tested according to the relevant specifications.

## LVDS DC Specifications

| Symbol      | Description  | Conditions                                       | Min   | Typ   | Max   | Units |
|-------------|--|--|-------|-------|-------|-------|
| $V_{CCO}$   | Supply voltage   |  | 2.375 | 2.5   | 2.625 | V     |
| $V_{OH}$    | Output High voltage for Q and $\bar{Q}$  | $R_T = 100\Omega$ across Q and $\bar{Q}$ signals | 1.25  | 1.425 | 1.6   | V     |
| $V_{OL}$    | Output Low voltage for Q and $\bar{Q}$   | $R_T = 100\Omega$ across Q and $\bar{Q}$ signals | 0.9   | 1.075 | 1.25  | V     |
| $V_{ODIFF}$ | Differential output voltage (Q – $\bar{Q}$ ),<br>Q = High or ( $\bar{Q} - Q$ ), $\bar{Q}$ = High | $R_T = 100\Omega$ across Q and $\bar{Q}$ signals | 250   | 350   | 450   | mV    |
| $V_{OCM}$   | Output common-mode voltage   | $R_T = 100\Omega$ across Q and $\bar{Q}$ signals | 1.125 | 1.25  | 1.375 | V     |
| $V_{IDIFF}$ | Differential input voltage (Q – $\bar{Q}$ ),<br>Q = High or ( $\bar{Q} - Q$ ), $\bar{Q}$ = High  | Common-mode input voltage = 1.25 V               | 100   | 350   | -     | mV    |
| $V_{ICM}$   | Input common-mode voltage  | Differential input voltage = $\pm 350$ mV        | 0.2   | 1.25  | 2.2   | V     |

### Notes:

1. Refer to Application Note [XAPP179](#) for termination schematics.

## LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a  $100\Omega$  differential load only. The  $V_{OH}$  levels are 200 mV below standard

LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

| DC Parameter               | Min  | Max   | Min  | Max   | Min  | Max   | Units |
|----------------------------|------|-------|------|-------|------|-------|-------|
| $V_{CCO}$                  | 3.0  |       | 3.3  |       | 3.6  |       | V     |
| $V_{OH}$                   | 1.8  | 2.11  | 1.92 | 2.28  | 2.13 | 2.41  | V     |
| $V_{OL}$                   | 0.96 | 1.27  | 1.06 | 1.43  | 1.30 | 1.57  | V     |
| $V_{IH}$                   | 1.49 | 2.72  | 1.49 | 2.72  | 1.49 | 2.72  | V     |
| $V_{IL}$                   | 0.86 | 2.125 | 0.86 | 2.125 | 0.86 | 2.125 | V     |
| Differential input voltage | 0.3  | -     | 0.3  | -     | 0.3  | -     | V     |

## Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRACE in the Xilinx Development System) and

back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-IIE devices unless otherwise noted.

### Global Clock Input to Output Delay for LVTTL, with DLL (Pin-to-Pin)<sup>(1)</sup>

| Symbol         | Description   | Speed Grade |     |     | Units |
|----------------|---|-------------|-----|-----|-------|
|                |   | All         | -7  | -6  |       |
|                |   | Min         | Max | Max |       |
| $T_{ICKOFDLL}$ | LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, with DLL. | 1.0         | 3.1 | 3.1 | ns    |

#### Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- Output timing is measured at 50%  $V_{CC}$  threshold with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables [Constants for Calculating  \$T\_{IOOP}\$](#)  and [Delay Measurement Methodology](#), page 11.
- DLL output jitter is already included in the timing calculation.
- For data *output* with different standards, adjust delays with the values shown in [IOB Output Delay Adjustments for Different Standards\(1\)](#), page 10. For a global clock input with standards other than LVTTL, adjust delays with values from the [I/O Standard Global Clock Input Adjustments](#), page 12.

### Global Clock Input to Output Delay for LVTTL, without DLL (Pin-to-Pin)<sup>(1)</sup>

| Symbol      | Description  | Device   | Speed Grade |     |     | Units |
|-------------|--|----------|-------------|-----|-----|-------|
|             |  |          | All         | -7  | -6  |       |
|             |  |          | Min         | Max | Max |       |
| $T_{ICKOF}$ | LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, without DLL. | XC2S50E  | 1.5         | 4.4 | 4.6 | ns    |
|             |  | XC2S100E | 1.5         | 4.4 | 4.6 | ns    |
|             |  | XC2S150E | 1.5         | 4.5 | 4.7 | ns    |
|             |  | XC2S200E | 1.5         | 4.5 | 4.7 | ns    |
|             |  | XC2S300E | 1.5         | 4.5 | 4.7 | ns    |
|             |  | XC2S400E | 1.5         | 4.6 | 4.8 | ns    |
|             |  | XC2S600E | 1.6         | 4.7 | 4.9 | ns    |

#### Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- Output timing is measured at 50%  $V_{CC}$  threshold with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables [Constants for Calculating  \$T\_{IOOP}\$](#)  and [Delay Measurement Methodology](#), page 11.
- For data *output* with different standards, adjust delays with the values shown in [IOB Output Delay Adjustments for Different Standards\(1\)](#), page 10. For a global clock input with standards other than LVTTL, adjust delays with values from the [I/O Standard Global Clock Input Adjustments](#), page 12.

### Global Clock Setup and Hold for LVTTTL Standard, *with* DLL (Pin-to-Pin)

| Symbol                  | Description  | Speed Grade |         | Units |
|-------------------------|--|-------------|---------|-------|
|                         |  | -7          | -6      |       |
|                         |  | Min         | Min     |       |
| $T_{PSDLL} / T_{PHDLL}$ | Input setup and hold time relative to global clock input signal for LVTTTL standard, no delay, IFF, <sup>(1)</sup> <i>with</i> DLL | 1.6 / 0     | 1.7 / 0 | ns    |

**Notes:**

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Delay Adjustments for Different Standards**, page 8. For a global clock input with standards other than LVTTTL, adjust delays with values from the **I/O Standard Global Clock Input Adjustments**, page 12.
5. A zero hold time listing indicates no hold time or a negative hold time.

### Global Clock Setup and Hold for LVTTTL Standard, *without* DLL (Pin-to-Pin)

| Symbol                | Description   | Device   | Speed Grade |         | Units |
|-----------------------|---|----------|-------------|---------|-------|
|                       |   |          | -7          | -6      |       |
|                       |   |          | Min         | Min     |       |
| $T_{PSFD} / T_{PHFD}$ | Input setup and hold time relative to global clock input signal for LVTTTL standard, no delay, IFF, <sup>(1)</sup> <i>without</i> DLL | XC2S50E  | 1.8 / 0     | 1.8 / 0 | ns    |
|                       |   | XC2S100E | 1.8 / 0     | 1.8 / 0 | ns    |
|                       |   | XC2S150E | 1.9 / 0     | 1.9 / 0 | ns    |
|                       |   | XC2S200E | 1.9 / 0     | 1.9 / 0 | ns    |
|                       |   | XC2S300E | 2.0 / 0     | 2.0 / 0 | ns    |
|                       |   | XC2S400E | 2.0 / 0     | 2.0 / 0 | ns    |
|                       |   | XC2S600E | 2.1 / 0     | 2.1 / 0 | ns    |

**Notes:**

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Delay Adjustments for Different Standards**, page 8. For a global clock input with standards other than LVTTTL, adjust delays with values from the **I/O Standard Global Clock Input Adjustments**, page 12.

## IOB Input Switching Characteristics<sup>(1)</sup>

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Delay Adjustments for Different Standards**, page 8.

| Symbol  | Description  | Device   | Speed Grade |     |            |     | Units |
|---|--|----------|-------------|-----|------------|-----|-------|
|   |  |          | -7          |     | -6         |     |       |
|   |  |          | Min         | Max | Min        | Max |       |
| <b>Propagation Delays</b>                         |  |          |             |     |            |     |       |
| $T_{IOPI}$  | Pad to I output, no delay                          | All      | 0.4         | 0.8 | 0.4        | 0.8 | ns    |
| $T_{IOPID}$                                       | Pad to I output, with delay                        | All      | 0.5         | 1.0 | 0.5        | 1.0 | ns    |
| $T_{IOPLI}$                                       | Pad to output IQ via transparent latch, no delay   | All      | 0.7         | 1.5 | 0.7        | 1.6 | ns    |
| $T_{IOPLID}$                                      | Pad to output IQ via transparent latch, with delay | XC2S50E  | 1.3         | 3.0 | 1.3        | 3.1 | ns    |
|   |  | XC2S100E | 1.3         | 3.0 | 1.3        | 3.1 | ns    |
|   |  | XC2S150E | 1.3         | 3.2 | 1.3        | 3.3 | ns    |
|   |  | XC2S200E | 1.3         | 3.2 | 1.3        | 3.3 | ns    |
|   |  | XC2S300E | 1.3         | 3.2 | 1.3        | 3.3 | ns    |
|   |  | XC2S400E | 1.4         | 3.2 | 1.4        | 3.4 | ns    |
|   |  | XC2S600E | 1.5         | 3.5 | 1.5        | 3.7 | ns    |
| <b>Sequential Delays</b>                          |  |          |             |     |            |     |       |
| $T_{IOCKIQ}$                                      | Clock CLK to output IQ                             | All      | 0.1         | 0.7 | 0.1        | 0.7 | ns    |
| <b>Setup/Hold Times with Respect to Clock CLK</b> |  |          |             |     |            |     |       |
| $T_{IOPICK} / T_{IOICKP}$                         | Pad, no delay                                      | All      | 1.4 / 0     | -   | 1.5 / 0    | -   | ns    |
| $T_{IOPICKD} / T_{IOICKPD}$                       | Pad, with delay                                    | XC2S50E  | 2.9 / 0     | -   | 2.9 / 0    | -   | ns    |
|   |  | XC2S100E | 2.9 / 0     | -   | 2.9 / 0    | -   | ns    |
|   |  | XC2S150E | 3.1 / 0     | -   | 3.1 / 0    | -   | ns    |
|   |  | XC2S200E | 3.1 / 0     | -   | 3.1 / 0    | -   | ns    |
|   |  | XC2S300E | 3.1 / 0     | -   | 3.1 / 0    | -   | ns    |
|   |  | XC2S400E | 3.2 / 0     | -   | 3.2 / 0    | -   | ns    |
|   |  | XC2S600E | 3.5 / 0     | -   | 3.5 / 0    | -   | ns    |
| $T_{IOICECK} / T_{IOICKICE}$                      | ICE input  | All      | 0.7 / 0.01  | -   | 0.7 / 0.01 | -   | ns    |
| <b>Set/Reset Delays</b>                           |  |          |             |     |            |     |       |
| $T_{IOSRCKI}$                                     | SR input (IFF, synchronous)                        | All      | 0.9         | -   | 1.0        | -   | ns    |
| $T_{IOSRIQ}$                                      | SR input to IQ (asynchronous)                      | All      | 0.5         | 1.2 | 0.5        | 1.4 | ns    |
| $T_{GSRQ}$  | GSR to output IQ                                   | All      | 3.8         | 8.5 | 3.8        | 9.7 | ns    |

### Notes:

- Input timing for LVTTTL is measured at 1.4V. For other I/O standards, see the table **Delay Measurement Methodology**, page 11.

## IOB Input Delay Adjustments for Different Standards

Input delays associated with the pad are specified for LVTTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol                              | Description                                    | Standard          | Speed Grade |       | Units |
|-------------------------------------|--|-------------------|-------------|-------|-------|
|                                     |  |                   | -7          | -6    |       |
| <b>Data Input Delay Adjustments</b> |  |                   |             |       |       |
| $T_{ILVTTTL}$                       | Standard-specific data input delay adjustments | LVTTTL            | 0           | 0     | ns    |
| $T_{ILVCMOS2}$                      |  | LVCMOS2           | 0           | 0     | ns    |
| $T_{ILVCMOS18}$                     |  | LVCMOS18          | 0.20        | 0.20  | ns    |
| $T_{ILVDS}$                         |  | LVDS              | 0.15        | 0.15  | ns    |
| $T_{ILVPECL}$                       |  | LVPECL            | 0.15        | 0.15  | ns    |
| $T_{I PCI33\_3}$                    |  | PCI, 33 MHz, 3.3V | 0.08        | 0.08  | ns    |
| $T_{I PCI66\_3}$                    |  | PCI, 66 MHz, 3.3V | -0.11       | -0.11 | ns    |
| $T_{IGTL}$                          |  | GTL               | 0.14        | 0.14  | ns    |
| $T_{IGTLP}$                         |  | GTL+              | 0.14        | 0.14  | ns    |
| $T_{IHSTL}$                         |  | HSTL              | 0.04        | 0.04  | ns    |
| $T_{ISSTL2}$                        |  | SSTL2             | 0.04        | 0.04  | ns    |
| $T_{ISSTL3}$                        |  | SSTL3             | 0.04        | 0.04  | ns    |
| $T_{ICTT}$                          |  | CTT               | 0.10        | 0.10  | ns    |
| $T_{IAGP}$                          |  | AGP               | 0.04        | 0.04  | ns    |



## IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Delay Adjustments for Different Standards(1)**, page 10.

| Symbol  | Description  | Speed Grade |     |         |     | Units |
|---|--|-------------|-----|---------|-----|-------|
|   |  | -7          |     | -6      |     |       |
|   |  | Min         | Max | Min     | Max |       |
| <b>Propagation Delays</b>                         |  |             |     |         |     |       |
| $T_{IOOP}$  | O input to pad   | 1.0         | 2.7 | 1.0     | 2.9 | ns    |
| $T_{IOOLP}$                                       | O input to pad via transparent latch                               | 1.2         | 3.1 | 1.2     | 3.4 | ns    |
| <b>3-state Delays</b>                             |  |             |     |         |     |       |
| $T_{IOTHZ}$                                       | T input to pad high impedance <sup>(1)</sup>                       | 0.7         | 1.7 | 0.7     | 1.9 | ns    |
| $T_{IOTON}$                                       | T input to valid data on pad                                       | 1.1         | 2.9 | 1.1     | 3.1 | ns    |
| $T_{IOTLPHZ}$                                     | T input to pad high impedance via transparent latch <sup>(1)</sup> | 0.8         | 2.0 | 0.8     | 2.2 | ns    |
| $T_{IOTLPON}$                                     | T input to valid data on pad via transparent latch                 | 1.2         | 3.2 | 1.2     | 3.4 | ns    |
| $T_{GTS}$   | GTS to pad high impedance <sup>(1)</sup>                           | 1.9         | 4.6 | 1.9     | 4.9 | ns    |
| <b>Sequential Delays</b>                          |  |             |     |         |     |       |
| $T_{IOCKP}$                                       | Clock CLK to pad   | 0.9         | 2.8 | 0.9     | 2.9 | ns    |
| $T_{IOCKHZ}$                                      | Clock CLK to pad high impedance (synchronous) <sup>(1)</sup>       | 0.7         | 2.0 | 0.7     | 2.2 | ns    |
| $T_{IOCKON}$                                      | Clock CLK to valid data on pad (synchronous)                       | 1.1         | 3.2 | 1.1     | 3.4 | ns    |
| <b>Setup/Hold Times with Respect to Clock CLK</b> |  |             |     |         |     |       |
| $T_{IOOCK} / T_{IOCKO}$                           | O input  | 1.0 / 0     | -   | 1.1 / 0 | -   | ns    |
| $T_{IOOCECK} / T_{IOCKOCE}$                       | OCE input  | 0.7 / 0     | -   | 0.7 / 0 | -   | ns    |
| $T_{IOSRCKO} / T_{IOCKOSR}$                       | SR input (OFF)   | 0.9 / 0     | -   | 1.0 / 0 | -   | ns    |
| $T_{IOTCK} / T_{IOCKT}$                           | 3-state setup times, T input                                       | 0.6 / 0     | -   | 0.7 / 0 | -   | ns    |
| $T_{IOTCECK} / T_{IOCKTCE}$                       | 3-state setup times, TCE input                                     | 0.6 / 0     | -   | 0.8 / 0 | -   | ns    |
| $T_{IOSRCKT} / T_{IOCKTSR}$                       | 3-state setup times, SR input (TFF)                                | 0.9 / 0     | -   | 1.0 / 0 | -   | ns    |
| <b>Set/Reset Delays</b>                           |  |             |     |         |     |       |
| $T_{IOSRP}$                                       | SR input to pad (asynchronous)                                     | 1.2         | 3.3 | 1.2     | 3.5 | ns    |
| $T_{IOSRHZ}$                                      | SR input to pad high impedance (asynchronous) <sup>(1)</sup>       | 1.0         | 2.4 | 1.0     | 2.7 | ns    |
| $T_{IOSRON}$                                      | SR input to valid data on pad (asynchronous)                       | 1.4         | 3.7 | 1.4     | 3.9 | ns    |
| $T_{IOGSRQ}$                                      | GSR to pad   | 3.8         | 8.5 | 3.8     | 9.7 | ns    |

### Notes:

1. Three-state turn-off delays should not be adjusted.

## IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol                                | Description  | Standard           | Speed Grade |       | Units |
|---------------------------------------|--|--------------------|-------------|-------|-------|
|                                       |  |                    | -7          | -6    |       |
| <b>Output Delay Adjustments (Adj)</b> |  |                    |             |       |       |
| $T_{OLVTTTL\_S2}$                     | Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, $C_{SL}$ ) | LVTTTL, Slow, 2 mA | 14.7        | 14.7  | ns    |
| $T_{OLVTTTL\_S4}$                     |  | 4 mA               | 7.5         | 7.5   | ns    |
| $T_{OLVTTTL\_S6}$                     |  | 6 mA               | 4.8         | 4.8   | ns    |
| $T_{OLVTTTL\_S8}$                     |  | 8 mA               | 3.0         | 3.0   | ns    |
| $T_{OLVTTTL\_S12}$                    |  | 12 mA              | 1.9         | 1.9   | ns    |
| $T_{OLVTTTL\_S16}$                    |  | 16 mA              | 1.7         | 1.7   | ns    |
| $T_{OLVTTTL\_S24}$                    |  | 24 mA              | 1.3         | 1.3   | ns    |
| $T_{OLVTTTL\_F2}$                     |  | LVTTTL, Fast, 2 mA | 13.1        | 13.1  | ns    |
| $T_{OLVTTTL\_F4}$                     |  | 4 mA               | 5.3         | 5.3   | ns    |
| $T_{OLVTTTL\_F6}$                     |  | 6 mA               | 3.1         | 3.1   | ns    |
| $T_{OLVTTTL\_F8}$                     |  | 8 mA               | 1.0         | 1.0   | ns    |
| $T_{OLVTTTL\_F12}$                    |  | 12 mA              | 0           | 0     | ns    |
| $T_{OLVTTTL\_F16}$                    |  | 16 mA              | -0.05       | -0.05 | ns    |
| $T_{OLVTTTL\_F24}$                    |  | 24 mA              | -0.20       | -0.20 | ns    |
| $T_{OLVCMOS2}$                        |  | LVC MOS2           | 0.09        | 0.09  | ns    |
| $T_{OLVCMOS18}$                       |  | LVC MOS18          | 0.7         | 0.7   | ns    |
| $T_{OLVDS}$                           |  | LVDS               | -1.2        | -1.2  | ns    |
| $T_{OLVPECL}$                         |  | LVPECL             | -0.41       | -0.41 | ns    |
| $T_{OPCI33\_3}$                       |  | PCI, 33 MHz, 3.3V  | 2.3         | 2.3   | ns    |
| $T_{OPCI66\_3}$                       |  | PCI, 66 MHz, 3.3V  | -0.41       | -0.41 | ns    |
| $T_{OGTL}$                            |  | GTL                | 0.49        | 0.49  | ns    |
| $T_{OGTLP}$                           |  | GTL+               | 0.8         | 0.8   | ns    |
| $T_{OHSTL\_I}$                        |  | HSTL I             | -0.51       | -0.51 | ns    |
| $T_{OHSTL\_III}$                      |  | HSTL III           | -0.91       | -0.91 | ns    |
| $T_{OHSTL\_IV}$                       | HSTL IV  | -1.01              | -1.01       | ns    |       |
| $T_{OSSTL2\_I}$                       | SSTL2 I  | -0.51              | -0.51       | ns    |       |
| $T_{OSSTL2\_II}$                      | SSTL2 II   | -0.91              | -0.91       | ns    |       |
| $T_{OSSTL3\_I}$                       | SSTL3 I  | -0.51              | -0.51       | ns    |       |
| $T_{OSSTL3\_II}$                      | SSTL3 II   | -1.01              | -1.01       | ns    |       |
| $T_{OCTT}$                            | CTT  | -0.61              | -0.61       | ns    |       |
| $T_{OAGP}$                            | AGP  | -0.91              | -0.91       | ns    |       |

### Notes:

- Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTTL. For other I/O standards and different loads, see the tables **Constants for Calculating  $T_{IOP}$**  and **Delay Measurement Methodology**, page 11.

## Calculation of $T_{IOOP}$ as a Function of Capacitance

$T_{IOOP}$  is the propagation delay from the O Input of the IOB to the pad. The values for  $T_{IOOP}$  are based on the standard capacitive load ( $C_{SL}$ ) for each I/O standard as listed in the table **Constants for Calculating  $T_{IOOP}$** , below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay,  $T_{IOOP1}$ .

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

Adj is selected from **IOB Output Delay Adjustments for Different Standards(1)**, page 10, according to the I/O standard used

$C_{LOAD}$  is the capacitive load for the design

$F_L$  is the capacitance scaling factor

## Delay Measurement Methodology

| Standard       | $V_L^{(1)}$                      | $V_H^{(1)}$                      | Meas. Point | $V_{REF}$ Typ <sup>(2)</sup> |
|----------------|----------------------------------|----------------------------------|-------------|------------------------------|
| LVTTL          | 0                                | 3                                | 1.4         | -                            |
| LVC MOS2       | 0                                | 2.5                              | 1.125       | -                            |
| PCI33_3        | Per PCI Spec                     |                                  |             | -                            |
| PCI66_3        | Per PCI Spec                     |                                  |             | -                            |
| GTL            | $V_{REF} - 0.2$                  | $V_{REF} + 0.2$                  | $V_{REF}$   | 0.80                         |
| GTL+           | $V_{REF} - 0.2$                  | $V_{REF} + 0.2$                  | $V_{REF}$   | 1.0                          |
| HSTL Class I   | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$   | 0.75                         |
| HSTL Class III | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$   | 0.90                         |
| HSTL Class IV  | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$   | 0.90                         |
| SSTL3 I and II | $V_{REF} - 1.0$                  | $V_{REF} + 1.0$                  | $V_{REF}$   | 1.5                          |
| SSTL2 I and II | $V_{REF} - 0.75$                 | $V_{REF} + 0.75$                 | $V_{REF}$   | 1.25                         |
| CTT            | $V_{REF} - 0.2$                  | $V_{REF} + 0.2$                  | $V_{REF}$   | 1.5                          |
| AGP            | $V_{REF} - (0.2 \times V_{CCO})$ | $V_{REF} + (0.2 \times V_{CCO})$ | $V_{REF}$   | Per AGP Spec                 |
| LVDS           | $1.2 - 0.125$                    | $1.2 + 0.125$                    | 1.2         |                              |
| LVPECL         | $1.6 - 0.3$                      | $1.6 + 0.3$                      | 1.6         |                              |

### Notes:

- Input waveform switches between  $V_L$  and  $V_H$ .
- Measurements are made at  $V_{REF}$  Typ, Maximum, and Minimum. Worst-case values are reported.
- I/O parameter measurements are made with the capacitance values shown in the following table, **Constants for Calculating  $T_{IOOP}$** . Refer to Application Note [XAPP179](#) for appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Constants for Calculating $T_{IOOP}$

| Standard                          | $C_{SL}^{(1)}$ (pF) | $F_L$ (ns/pF) |
|-----------------------------------|---------------------|---------------|
| LVTTL Fast Slew Rate, 2 mA drive  | 35                  | 0.41          |
| LVTTL Fast Slew Rate, 4 mA drive  | 35                  | 0.20          |
| LVTTL Fast Slew Rate, 6 mA drive  | 35                  | 0.13          |
| LVTTL Fast Slew Rate, 8 mA drive  | 35                  | 0.079         |
| LVTTL Fast Slew Rate, 12 mA drive | 35                  | 0.044         |
| LVTTL Fast Slew Rate, 16 mA drive | 35                  | 0.043         |
| LVTTL Fast Slew Rate, 24 mA drive | 35                  | 0.033         |
| LVTTL Slow Slew Rate, 2 mA drive  | 35                  | 0.41          |
| LVTTL Slow Slew Rate, 4 mA drive  | 35                  | 0.20          |
| LVTTL Slow Slew Rate, 6 mA drive  | 35                  | 0.100         |
| LVTTL Slow Slew Rate, 8 mA drive  | 35                  | 0.086         |
| LVTTL Slow Slew Rate, 12 mA drive | 35                  | 0.058         |
| LVTTL Slow Slew Rate, 16 mA drive | 35                  | 0.050         |
| LVTTL Slow Slew Rate, 24 mA drive | 35                  | 0.048         |
| LVC MOS2                          | 35                  | 0.041         |
| LVC MOS18                         | 35                  | 0.050         |
| PCI 33 MHz 3.3V                   | 10                  | 0.050         |
| PCI 66 MHz 3.3V                   | 10                  | 0.033         |
| GTL                               | 0                   | 0.014         |
| GTL+                              | 0                   | 0.017         |
| HSTL Class I                      | 20                  | 0.022         |
| HSTL Class III                    | 20                  | 0.016         |
| HSTL Class IV                     | 20                  | 0.014         |
| SSTL2 Class I                     | 30                  | 0.028         |
| SSTL2 Class II                    | 30                  | 0.016         |
| SSTL3 Class I                     | 30                  | 0.029         |
| SSTL3 Class II                    | 30                  | 0.016         |
| CTT                               | 20                  | 0.035         |
| AGP                               | 10                  | 0.037         |

### Notes:

- I/O parameter measurements are made with the capacitance values shown above. Refer to Application Note [XAPP179](#) for appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Clock Distribution Switching Characteristics

$T_{GPIO}$  is specified for LVTTTL levels. For other standards, adjust  $T_{GPIO}$  with the values shown in **I/O Standard Global Clock Input Adjustments**.

| Symbol                     | Description                             | Speed Grade |     | Units |
|----------------------------|---|-------------|-----|-------|
|                            |   | -7          | -6  |       |
|                            |   | Max         | Max |       |
| <b>GCLK IOB and Buffer</b> |   |             |     |       |
| $T_{GPIO}$                 | Global clock pad to output              | 0.7         | 0.7 | ns    |
| $T_{GIO}$                  | Global clock buffer I input to O output | 0.45        | 0.5 | ns    |

## I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol                              | Description  | Standard          | Speed Grade |       | Units |
|-------------------------------------|--|-------------------|-------------|-------|-------|
|                                     |  |                   | -7          | -6    |       |
| <b>Data Input Delay Adjustments</b> |  |                   |             |       |       |
| $T_{GPLVTTL}$                       | Standard-specific global clock input delay adjustments | LVTTTL            | 0           | 0     | ns    |
| $T_{GPLVCMOS2}$                     |  | LVCOS2            | 0           | 0     | ns    |
| $T_{GPLVCMOS18}$                    |  | LVCOS18           | 0.2         | 0.2   | ns    |
| $T_{GPLVCDS}$                       |  | LVDS              | 0.38        | 0.38  | ns    |
| $T_{GPLVPECL}$                      |  | LVCPECL           | 0.38        | 0.38  | ns    |
| $T_{GPPCI33_3}$                     |  | PCI, 33 MHz, 3.3V | 0.08        | 0.08  | ns    |
| $T_{GPPCI66_3}$                     |  | PCI, 66 MHz, 3.3V | -0.11       | -0.11 | ns    |
| $T_{GPGTL}$                         |  | GTL               | 0.37        | 0.37  | ns    |
| $T_{GPGTLP}$                        |  | GTL+              | 0.37        | 0.37  | ns    |
| $T_{GPHSTL}$                        |  | HSTL              | 0.27        | 0.27  | ns    |
| $T_{GPSSTL2}$                       |  | SSTL2             | 0.27        | 0.27  | ns    |
| $T_{GPSSTL3}$                       |  | SSTL3             | 0.27        | 0.27  | ns    |
| $T_{GPCTT}$                         |  | CTT               | 0.33        | 0.33  | ns    |
| $T_{GPAGP}$                         |  | AGP               | 0.27        | 0.27  | ns    |

### Notes:

- Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table **Delay Measurement Methodology**, page 11.

## DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect

worst-case values across the recommended operating conditions.

| Symbol        | Description                      | $F_{CLKIN}$    | Speed Grade |     |     |     | Units |
|---------------|----------------------------------|----------------|-------------|-----|-----|-----|-------|
|               |                                  |                | -7          |     | -6  |     |       |
|               |                                  |                | Min         | Max | Min | Max |       |
| $F_{CLKINHF}$ | Input clock frequency (CLKDLLHF) | -              | 60          | 320 | 60  | 275 | MHz   |
| $F_{CLKINLF}$ | Input clock frequency (CLKDLL)   | -              | 25          | 160 | 25  | 135 | MHz   |
| $T_{DLLPW}$   | Input clock pulse width          | $\geq 25$ MHz  | 5.0         | -   | 5.0 | -   | ns    |
|               |                                  | $\geq 50$ MHz  | 3.0         | -   | 3.0 | -   | ns    |
|               |                                  | $\geq 100$ MHz | 2.4         | -   | 2.4 | -   | ns    |
|               |                                  | $\geq 150$ MHz | 2.0         | -   | 2.0 | -   | ns    |
|               |                                  | $\geq 200$ MHz | 1.8         | -   | 1.8 | -   | ns    |
|               |                                  | $\geq 250$ MHz | 1.5         | -   | 1.5 | -   | ns    |
|               |                                  | $\geq 300$ MHz | 1.3         | -   | NA  | -   |       |

## DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

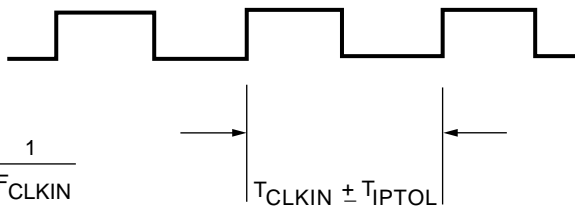
Figure 1, page 14, provides definitions for various parameters in the table below.

| Symbol       | Description  | $F_{CLKIN}$ | CLKDLLHF |           | CLKDLL |           | Units   |
|--------------|--|-------------|----------|-----------|--------|-----------|---------|
|              |  |             | Min      | Max       | Min    | Max       |         |
| $T_{IPTOL}$  | Input clock period tolerance   |             | -        | 1.0       | -      | 1.0       | ns      |
| $T_{IJITCC}$ | Input clock jitter tolerance (cycle-to-cycle)                          |             | -        | $\pm 150$ | -      | $\pm 300$ | ps      |
| $T_{LOCK}$   | Time required for DLL to acquire lock <sup>(1)</sup>                   | $> 60$ MHz  | -        | 20        | -      | 20        | $\mu$ s |
|              |  | 50-60 MHz   | -        | -         | -      | 25        | $\mu$ s |
|              |  | 40-50 MHz   | -        | -         | -      | 50        | $\mu$ s |
|              |  | 30-40 MHz   | -        | -         | -      | 90        | $\mu$ s |
|              |  | 25-30 MHz   | -        | -         | -      | 120       | $\mu$ s |
| $T_{OJITCC}$ | Output jitter (cycle-to-cycle) for any DLL clock output <sup>(2)</sup> |             | -        | $\pm 60$  | -      | $\pm 60$  | ps      |
| $T_{PHIO}$   | Phase offset between CLKIN and CLKO <sup>(3)</sup>                     |             | -        | $\pm 100$ | -      | $\pm 100$ | ps      |
| $T_{PHOO}$   | Phase offset between clock outputs on the DLL <sup>(4)</sup>           |             | -        | $\pm 140$ | -      | $\pm 140$ | ps      |
| $T_{PHIOM}$  | Phase difference between CLKIN and CLKO <sup>(5)</sup>                 |             | -        | $\pm 160$ | -      | $\pm 160$ | ps      |
| $T_{PHOOM}$  | Phase difference between clock outputs on the DLL <sup>(6)</sup>       |             | -        | $\pm 200$ | -      | $\pm 200$ | ps      |

### Notes:

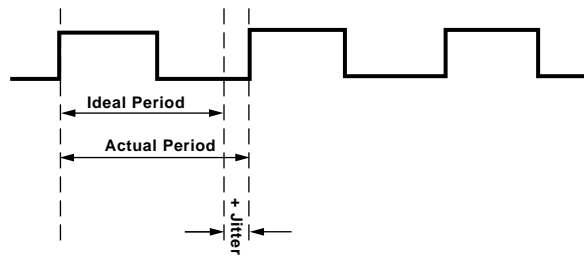
- Commercial operating conditions. Add 30% for Industrial operating conditions.
- Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
- Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
- Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* output jitter and input clock jitter.
- Maximum Phase Difference between CLKIN and CLKO** is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
- Maximum Phase Difference between Clock Outputs on the DLL** is the sum of output jitter and phase offset between any two DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

**Period Tolerance:** the allowed input clock period change in nanoseconds.

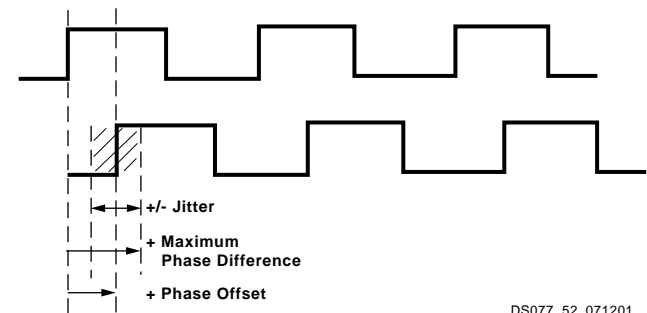
$$T_{\text{CLKIN}} = \frac{1}{F_{\text{CLKIN}}}$$


$T_{\text{CLKIN}} \pm T_{\text{IPTOL}}$

**Output Jitter:** the difference between an ideal reference clock edge and the actual design.



**Phase Offset and Maximum Phase Difference**



DS077\_52\_071201

Figure 1: Period Tolerance and Clock Jitter

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Symbol  | Description  | Speed Grade |      |         |      | Units |
|---|--|-------------|------|---------|------|-------|
|   |  | -7          |      | -6      |      |       |
|   |  | Min         | Max  | Min     | Max  |       |
| <b>Combinatorial Delays</b>                       |  |             |      |         |      |       |
| $T_{ILO}$   | 4-input function: F/G inputs to X/Y outputs                          | 0.18        | 0.42 | 0.18    | 0.47 | ns    |
| $T_{IF5}$   | 5-input function: F/G inputs to F5 output                            | 0.3         | 0.8  | 0.3     | 0.9  | ns    |
| $T_{IF5X}$  | 5-input function: F/G inputs to X output                             | 0.3         | 0.8  | 0.3     | 0.9  | ns    |
| $T_{IF6Y}$  | 6-input function: F/G inputs to Y output via F6 MUX                  | 0.3         | 0.9  | 0.3     | 1.0  | ns    |
| $T_{F5INY}$                                       | 6-input function: F5IN input to Y output                             | 0.04        | 0.2  | 0.04    | 0.22 | ns    |
| $T_{IFNCTL}$                                      | Incremental delay routing through transparent latch to XQ/YQ outputs | -           | 0.7  | -       | 0.8  | ns    |
| $T_{BYBY}$  | BY input to YB output  | 0.18        | 0.46 | 0.18    | 0.51 | ns    |
| <b>Sequential Delays</b>                          |  |             |      |         |      |       |
| $T_{CKO}$   | FF clock CLK to XQ/YQ outputs  | 0.3         | 0.9  | 0.3     | 1.0  | ns    |
| $T_{CKLO}$  | Latch clock CLK to XQ/YQ outputs                                     | 0.3         | 0.9  | 0.3     | 1.0  | ns    |
| <b>Setup/Hold Times with Respect to Clock CLK</b> |  |             |      |         |      |       |
| $T_{ICK} / T_{CKI}$                               | 4-input function: F/G inputs   | 1.0 / 0     | -    | 1.1 / 0 | -    | ns    |
| $T_{IF5CK} / T_{CKIF5}$                           | 5-input function: F/G inputs   | 1.4 / 0     | -    | 1.5 / 0 | -    | ns    |
| $T_{F5INCK} / T_{CKF5IN}$                         | 6-input function: F5IN input   | 0.8 / 0     | -    | 0.8 / 0 | -    | ns    |
| $T_{IF6CK} / T_{CKIF6}$                           | 6-input function: F/G inputs via F6 MUX                              | 1.5 / 0     | -    | 1.6 / 0 | -    | ns    |
| $T_{DICK} / T_{CKDI}$                             | BX/BY inputs   | 0.7 / 0     | -    | 0.8 / 0 | -    | ns    |
| $T_{CECK} / T_{CKCE}$                             | CE input   | 0.7 / 0     | -    | 0.7 / 0 | -    | ns    |
| $T_{RCK} / T_{CKR}$                               | SR/BY inputs (synchronous)   | 0.52 / 0    | -    | 0.6 / 0 | -    | ns    |
| <b>Clock CLK</b>                                  |  |             |      |         |      |       |
| $T_{CH}$  | Pulse width, High  | 1.3         | -    | 1.4     | -    | ns    |
| $T_{CL}$  | Pulse width, Low   | 1.3         | -    | 1.4     | -    | ns    |
| <b>Set/Reset</b>                                  |  |             |      |         |      |       |
| $T_{RPW}$   | Pulse width, SR/BY inputs  | 2.1         | -    | 2.4     | -    | ns    |
| $T_{RQ}$  | Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)              | 0.3         | 0.9  | 0.3     | 1.0  | ns    |
| $F_{TOG}$   | Toggle frequency (for export control)                                | -           | 400  | -       | 357  | MHz   |

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

| Symbol  | Description                                | Speed Grade |      |         |      | Units |
|---|--|-------------|------|---------|------|-------|
|   |  | -7          |      | -6      |      |       |
|   |  | Min         | Max  | Min     | Max  |       |
| <b>Combinatorial Delays</b>                       |  |             |      |         |      |       |
| $T_{OPX}$   | F operand inputs to X via XOR              | -           | 0.8  | -       | 0.8  | ns    |
| $T_{OPXB}$  | F operand input to XB output               | -           | 0.8  | -       | 0.9  | ns    |
| $T_{OPY}$   | F operand input to Y via XOR               | -           | 1.4  | -       | 1.5  | ns    |
| $T_{OPYB}$  | F operand input to YB output               | -           | 1.1  | -       | 1.3  | ns    |
| $T_{OPCYF}$                                       | F operand input to COUT output             | -           | 0.9  | -       | 1.0  | ns    |
| $T_{OPGY}$  | G operand inputs to Y via XOR              | -           | 0.8  | -       | 0.9  | ns    |
| $T_{OPGYB}$                                       | G operand input to YB output               | -           | 1.2  | -       | 1.3  | ns    |
| $T_{OPCYG}$                                       | G operand input to COUT output             | -           | 0.9  | -       | 1.0  | ns    |
| $T_{BXCX}$  | BX initialization input to COUT            | -           | 0.51 | -       | 0.6  | ns    |
| $T_{CINX}$  | CIN input to X output via XOR              | -           | 0.6  | -       | 0.7  | ns    |
| $T_{CINXB}$                                       | CIN input to XB                            | -           | 0.07 | -       | 0.1  | ns    |
| $T_{CINY}$  | CIN input to Y via XOR                     | -           | 0.7  | -       | 0.7  | ns    |
| $T_{CINYB}$                                       | CIN input to YB                            | -           | 0.4  | -       | 0.5  | ns    |
| $T_{BYC}$   | CIN input to COUT output                   | -           | 0.14 | -       | 0.15 | ns    |
| <b>Multiplier Operation</b>                       |  |             |      |         |      |       |
| $T_{FANDXB}$                                      | F1/2 operand inputs to XB output via AND   | -           | 0.35 | -       | 0.4  | ns    |
| $T_{FANDYB}$                                      | F1/2 operand inputs to YB output via AND   | -           | 0.7  | -       | 0.8  | ns    |
| $T_{FANDCY}$                                      | F1/2 operand inputs to COUT output via AND | -           | 0.5  | -       | 0.6  | ns    |
| $T_{GANDYB}$                                      | G1/2 operand inputs to YB output via AND   | -           | 0.6  | -       | 0.7  | ns    |
| $T_{GANDCY}$                                      | G1/2 operand inputs to COUT output via AND | -           | 0.3  | -       | 0.4  | ns    |
| <b>Setup/Hold Times with Respect to Clock CLK</b> |  |             |      |         |      |       |
| $T_{CCKX} / T_{CKCX}$                             | CIN input to FFX                           | 1.2 / 0     | -    | 1.3 / 0 | -    | ns    |
| $T_{CCKY} / T_{CKCY}$                             | CIN input to FFY                           | 1.2 / 0     | -    | 1.3 / 0 | -    | ns    |



## CLB Distributed RAM Switching Characteristics

| Symbol  | Description                                       | Speed Grade |     |         |     | Units |
|---|---|-------------|-----|---------|-----|-------|
|   |   | -7          |     | -6      |     |       |
|   |   | Min         | Max | Min     | Max |       |
| <b>Sequential Delays</b>                          |   |             |     |         |     |       |
| $T_{SHCKO16}$                                     | Clock CLK to X/Y outputs (WE active, 16 x 1 mode) | 0.6         | 1.5 | 0.6     | 1.7 | ns    |
| $T_{SHCKO32}$                                     | Clock CLK to X/Y outputs (WE active, 32 x 1 mode) | 0.8         | 1.9 | 0.8     | 2.1 | ns    |
| <b>Setup/Hold Times with Respect to Clock CLK</b> |   |             |     |         |     |       |
| $T_{AS} / T_{AH}$                                 | F/G address inputs                                | 0.42 / 0    | -   | 0.5 / 0 | -   | ns    |
| $T_{DS} / T_{DH}$                                 | BX/BY data inputs (DIN)                           | 0.53 / 0    | -   | 0.6 / 0 | -   | ns    |
| $T_{WS} / T_{WH}$                                 | CE input (WS)                                     | 0.7 / 0     | -   | 0.8 / 0 | -   | ns    |
| <b>Clock CLK</b>                                  |   |             |     |         |     |       |
| $T_{WPH}$   | Pulse width, High                                 | 2.1         | -   | 2.4     | -   | ns    |
| $T_{WPL}$   | Pulse width, Low                                  | 2.1         | -   | 2.4     | -   | ns    |
| $T_{WC}$  | Clock period to meet address write cycle time     | 4.2         | -   | 4.8     | -   | ns    |

## CLB Shift Register Switching Characteristics

| Symbol  | Description              | Speed Grade |     |         |     | Units |
|---|--------------------------|-------------|-----|---------|-----|-------|
|   |                          | -7          |     | -6      |     |       |
|   |                          | Min         | Max | Min     | Max |       |
| <b>Sequential Delays</b>                          |                          |             |     |         |     |       |
| $T_{REG}$   | Clock CLK to X/Y outputs | 1.2         | 2.9 | 1.2     | 3.2 | ns    |
| <b>Setup/Hold Times with Respect to Clock CLK</b> |                          |             |     |         |     |       |
| $T_{SHDICK}$                                      | BX/BY data inputs (DIN)  | 0.53 / 0    | -   | 0.6 / 0 | -   | ns    |
| $T_{SHCECK}$                                      | CE input (WS)            | 0.7 / 0     | -   | 0.8 / 0 | -   | ns    |
| <b>Clock CLK</b>                                  |                          |             |     |         |     |       |
| $T_{SRPH}$  | Pulse width, High        | 2.1         | -   | 2.4     | -   | ns    |
| $T_{SRPL}$  | Pulse width, Low         | 2.1         | -   | 2.4     | -   | ns    |

## Block RAM Switching Characteristics

| Symbol  | Description                                 | Speed Grade |     |         |     | Units |
|---|---|-------------|-----|---------|-----|-------|
|   |   | -7          |     | -6      |     |       |
|   |   | Min         | Max | Min     | Max |       |
| <b>Sequential Delays</b>                          |   |             |     |         |     |       |
| $T_{BCKO}$  | Clock CLK to DOUT output                    | 0.6         | 3.1 | 0.6     | 3.5 | ns    |
| <b>Setup/Hold Times with Respect to Clock CLK</b> |   |             |     |         |     |       |
| $T_{BACK} / T_{BCKA}$                             | ADDR inputs                                 | 1.0 / 0     | -   | 1.1 / 0 | -   | ns    |
| $T_{BDCK} / T_{BCKD}$                             | DIN inputs                                  | 1.0 / 0     | -   | 1.1 / 0 | -   | ns    |
| $T_{BECK} / T_{BCKE}$                             | EN inputs                                   | 2.2 / 0     | -   | 2.5 / 0 | -   | ns    |
| $T_{BRCK} / T_{BCKR}$                             | RST input                                   | 2.1 / 0     | -   | 2.3 / 0 | -   | ns    |
| $T_{BWCK} / T_{BCKW}$                             | WEN input                                   | 2.0 / 0     | -   | 2.2 / 0 | -   | ns    |
| <b>Clock CLK</b>                                  |   |             |     |         |     |       |
| $T_{BPWH}$  | Pulse width, High                           | 1.4         | -   | 1.5     | -   | ns    |
| $T_{BPWL}$  | Pulse width, Low                            | 1.4         | -   | 1.5     | -   | ns    |
| $T_{BCCS}$  | CLKA -> CLKB setup time for different ports | 2.7         | -   | 3.0     | -   | ns    |

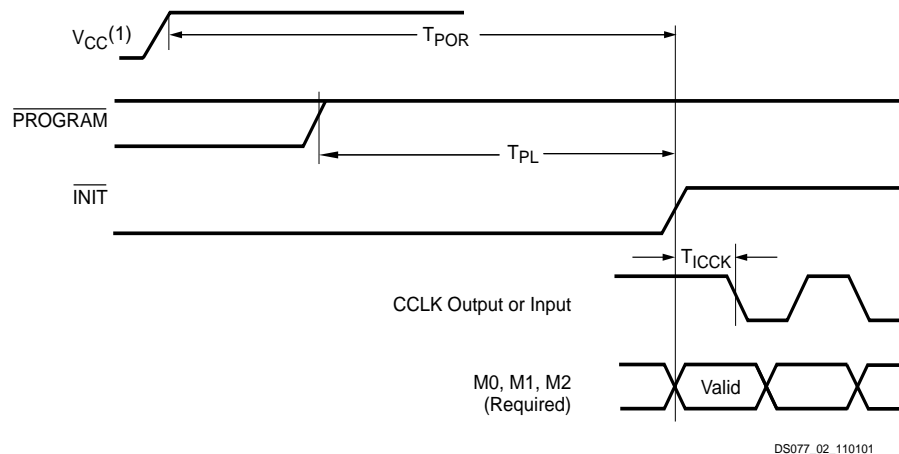
## TBUF Switching Characteristics

| Symbol    | Description                            | Speed Grade |      | Units |
|-----------|--|-------------|------|-------|
|           |  | -7          | -6   |       |
|           |  | Max         | Max  |       |
| $T_{IO}$  | IN input to OUT output                 | 0           | 0    | ns    |
| $T_{OFF}$ | TRI input to OUT output high impedance | 0.1         | 0.11 | ns    |
| $T_{ON}$  | TRI input to valid data on OUT output  | 0.1         | 0.11 | ns    |

## JTAG Test Access Port Switching Characteristics

| Symbol                                      | Description                               | Speed Grade |      |           |      | Units |
|---|---|-------------|------|-----------|------|-------|
|   |   | -7          |      | -6        |      |       |
|   |   | Min         | Max  | Min       | Max  |       |
| <b>Setup/Hold Times with Respect to TCK</b> |   |             |      |           |      |       |
| $T_{TAPTCK} / T_{TCKTAP}$                   | TMS and TDI setup times and hold times    | 4.0 / 2.0   | -    | 4.0 / 2.0 | -    | ns    |
| <b>Sequential Delays</b>                    |   |             |      |           |      |       |
| $T_{TCKTDO}$                                | Output delay from clock TCK to output TDO | -           | 11.0 | -         | 11.0 | ns    |
| $F_{TCK}$                                   | TCK clock frequency                       | -           | 33   | -         | 33   | MHz   |

## Configuration Switching Characteristics

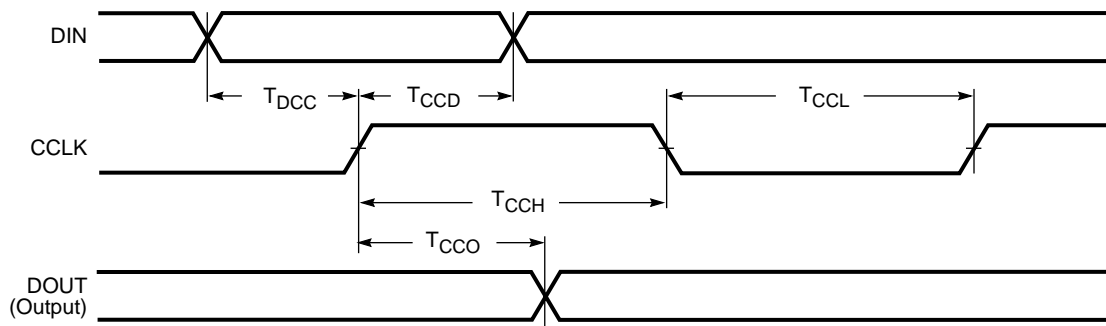


| Symbol        | Description                                 | All Devices |     | Units   |
|---------------|---|-------------|-----|---------|
|               |   | Min         | Max |         |
| $T_{POR}$     | Power-on reset                              | -           | 2   | ms      |
| $T_{PL}$      | Program latency                             | -           | 100 | $\mu$ s |
| $T_{ICCK}$    | CCLK output delay (Master serial mode only) | 0.5         | 4   | $\mu$ s |
| $T_{PROGRAM}$ | Program pulse width                         | 300         | -   | ns      |

### Notes:

- Before configuration can begin,  $V_{CCINT}$  and  $V_{CCO}$  Bank 2 must reach the recommended operating voltage.

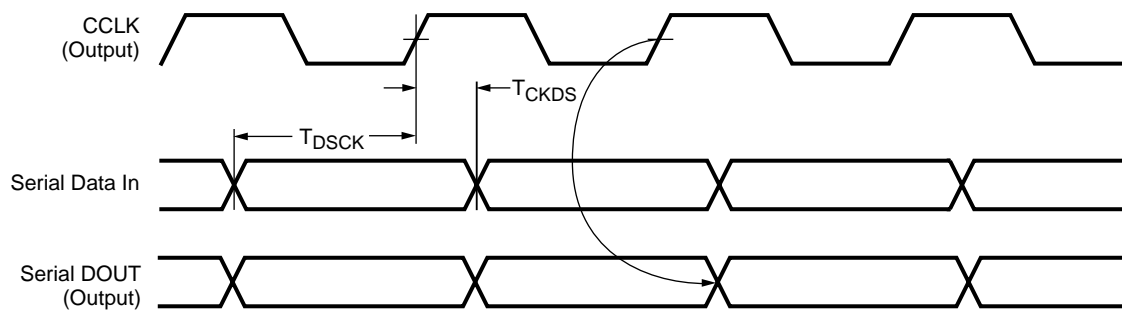
Figure 2: Configuration Timing on Power-Up



DS001\_16\_032300

| Symbol                              |      | Description       | All Devices |     | Units |
|-------------------------------------|------|-------------------|-------------|-----|-------|
|                                     |      |                   | Min         | Max |       |
| T <sub>DCC</sub> / T <sub>CCD</sub> | CCLK | DIN setup/hold    | 5 / 0       | -   | ns    |
| T <sub>CCO</sub>                    |      | DOUT              | -           | 12  | ns    |
| T <sub>CCH</sub>                    |      | High time         | 5           | -   | ns    |
| T <sub>CCL</sub>                    |      | Low time          | 5           | -   | ns    |
| F <sub>CC</sub>                     |      | Maximum frequency | -           | 66  | MHz   |

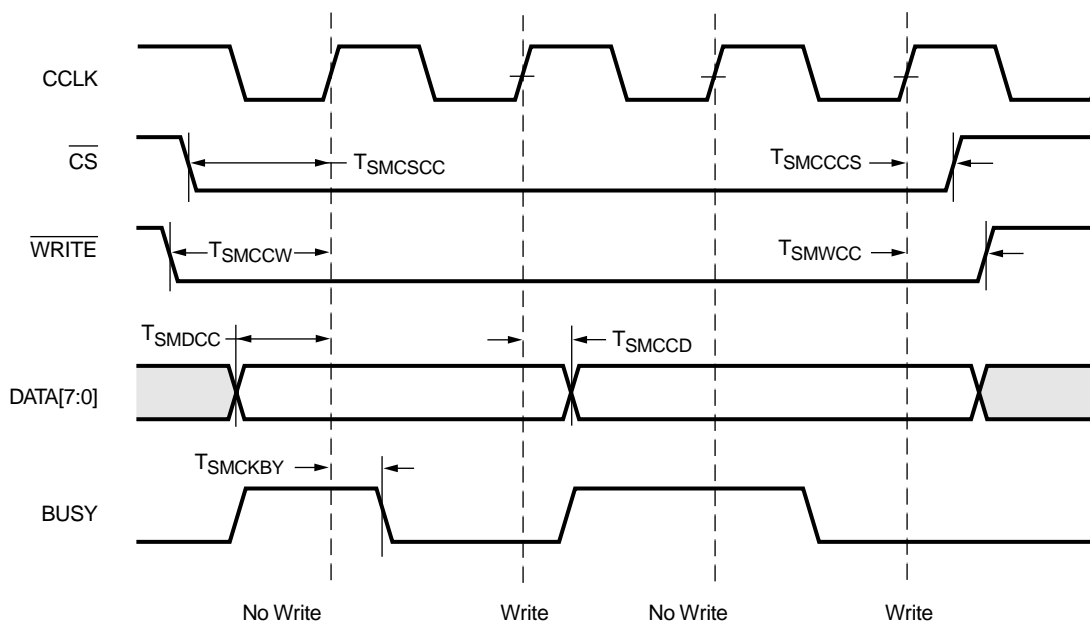
Figure 3: Slave Serial Mode Timing



DS001\_17\_032300

| Symbol                                |      | Description                                 | All Devices |      | Units |
|---------------------------------------|------|---|-------------|------|-------|
|                                       |      |   | Min         | Max  |       |
| T <sub>DSCK</sub> / T <sub>CKDS</sub> | CCLK | DIN setup/hold                              | 5 / 0       | -    | ns    |
| T <sub>CCO</sub>                      |      | DOUT  | -           | 12   | ns    |
| F <sub>CC</sub>                       |      | Frequency tolerance with respect to nominal | -30%        | +45% | -     |

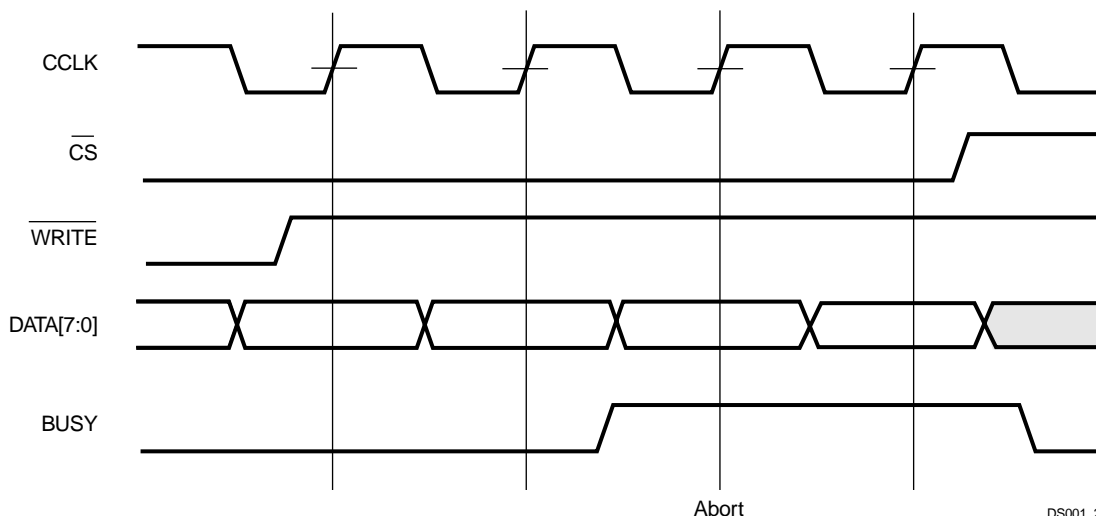
Figure 4: Master Serial Mode Timing



DS001\_20\_061200

| Symbol                      | Description                 | All Devices |     | Units |
|-----------------------------|-----------------------------|-------------|-----|-------|
|                             |                             | Min         | Max |       |
| $T_{SMDC}$ / $T_{SMCCD}$    | D0-D7 setup/hold            | 5 / 1       | -   | ns    |
| $T_{SMCSCC}$ / $T_{SMCCCS}$ | CS setup/hold               | 7 / 1       | -   | ns    |
| $T_{SMCCW}$ / $T_{SMWCC}$   | WRITE setup/hold            | 7 / 1       | -   | ns    |
| $T_{SMCKBY}$                | BUSY propagation delay      | -           | 12  | ns    |
| $F_{CC}$                    | Frequency                   | -           | 66  | MHz   |
| $F_{CCNH}$                  | Frequency with no handshake | -           | 50  | MHz   |

Figure 5: Slave Parallel (SelectMAP) Mode Write Timing



DS001\_21\_032300

Figure 6: Slave Parallel (SelectMAP) Mode Write Abort Waveforms

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## Revision History

| Version No. | Date     | Description   |
|-------------|----------|---|
| 1.0         | 11/15/01 | Initial Xilinx release.   |
| 1.1         | 06/28/02 | Added -7 speed grade and extended DLL specs to Industrial.  |
| 2.0         | 11/18/02 | Added XC2S400E and XC2S600E. Added minimum specifications. Added note to I/O leakage spec. Added reference to XAPP450 for Power-On Requirements. Removed Preliminary designation. |

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## The Spartan-IIE Family Data Sheet

DS077-1, *Spartan-IIE 1.8V FPGA Family: [Introduction and Ordering Information](#)* (Module 1)

DS077-2, *Spartan-IIE 1.8V FPGA Family: [Functional Description](#)* (Module 2)

DS077-3, *Spartan-IIE 1.8V FPGA Family: **DC and Switching Characteristics*** (Module 3)

DS077-4, *Spartan-IIE 1.8V FPGA Family: [Pinout Tables](#)* (Module 4)