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Foundation IP for 7nm FinFETs: Design and Implementation

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Introduction

Four years following the introduction of the first generation FinFETs, the 22nm Tri-Gate, and roughly one year after the first production shipments of 14/16nm FinFETs, 10nm FinFET designs are taping out and are slated for production in 2016. Fundamental research on 7nm FinFET technology started in 2013 and today the design and EDA communities are preparing the infrastructure for designing in 7nm FinFETs. For all designers, the 7nm node promises to deliver significant area gains from the 10nm node and to exploit the cumulative experience in the lithography and reliability aspects gained in the development of the first three generations of FinFETs. As memory content can consume more than 50 percent of the system-on-chip (SoC) area, successful integration of memory in advanced-node SoCs requires a clear understanding of the FinFET architecture and its challenges.

Benefits and Challenges of 7nm Process

Initial logic development for the 14/16nm node was challenging on many fronts. The new 3D device architecture brings higher parasitics, tighter interconnect pitch, higher negative-bias temperature instability (NBTI) and complex time-dependent dielectric breakdown (TDDB) reliability challenges, and a more complex gate stack topology. In addition to the inherent issues in 3D FinFET design, the 14/16nm node has undergone several iterations to provide significant performance and reliability improvements.

While the 10nm node builds on the experiences of 14/16nm, process designers quickly realized that they could push the technology past 10nm to 7nm for a significant area benefit. However, the lithography and reliability challenges associated with the 7nm node are not to be underestimated. The smaller node requires triple and quadruple pattering for critical layers, mechanical stability of narrower fins and the careful design of active area and gate interconnects to mitigate higher interconnect resistance stemming from tighter pitches, which can increase intra-die variability. As the EDA and design communities gear up for the 7nm node, progress in surmounting those challenges has been amazingly fast.

Intra-Die Variability and the Design of Foundation IP

Triple and quadruple pattering for critical layers of the 7nm devices and tighter pitches of fins and interconnect will result in an increase in intra-die variability. Dealing with the increased intra-die variability is going to be challenging for IP design in general and for the design of SRAM memories in particular. Designing robust SRAMs covering 6-sigma variability across process corners will require on-chip sensing and compensation in addition to creative assist circuits. Low voltage operation for power saving will exacerbate these challenges.

The tighter pitch and interconnect shown in Figure 1 brings a significant increase in parasitics, making efficient routing in memory and library architecture critical. Figure 1 shows 2D (left) and 3D (right) examples of a simulated footprint of a 10-track high 2-input NAND standard cell implemented with 7nm strained silicon FinFETs, quadruple spacer transfer fin patterning, double spacer transfer gate patterning

and quadruple LELELELE M0 and M1 patterning. To design robust SoCs in 7nm, designers must rely on thoroughly and accurately modeled standard cells and memory blocks that account for all the intricate details associated with the full implementation, from digitizing to silicon realization.
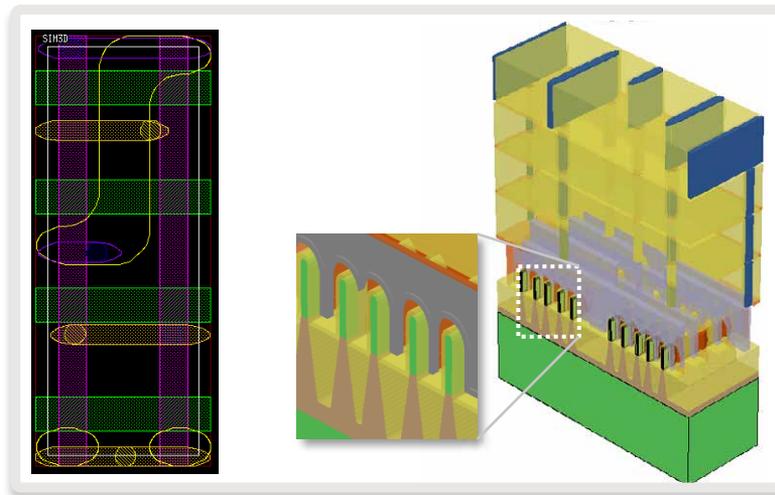

Figure 1. Simulated footprint (left) and 3D visualization (right) of a 7nm 2-input NAND gate

Extensive reliability simulation and analysis are more critical due to the increased complexities from to electromigration (EM), TDDB, and NBTI. The tighter interconnect pitches and narrower metal wires shown in Figure 1 bring a higher risk of early EM failure. TDDB and NBTI are also risks in advanced nodes. In addition to the risk of early EM failures, tighter pitches can bring an increase in device and interconnect parasitics. Designers must carefully simulate critical paths with good TDDB and NBTI models to accurately assess and mitigate potential performance and reliability failures stemming from NBTI and TDDB.

Reliability at the 7nm Node

The reliability concerns of the 7nm node are no different than at 10nm or 14/16nm. But the narrower interconnect EM and self-heating issues amplifies concerns. TDDB, NBTI, hot carrier injection (HCI), electrostatic discharge (ESD), and soft errors will be treated the same way as in previous nodes, but as the parameters shrink, designers will require more accurate modeling and simulations.

The thermal modeling of devices for self-heating analysis in the proximity of blocks with different temperature profiles is one area where more accurate modeling is required. In addition, modeling within the ambit of the specific SoC blocks can greatly affect accuracy. Figure 2 shows an example TCAD simulation of the thermal profile of a critical mixed-signal/analog circuit requiring device matching in the presence of neighbors with different thermal profiles, with one fin rising vertically from the 0 horizontal axis to 1.5μm and the plane extending to the right for 2μm. Even within this small example area, the variation in temperature is not simply correlated to active (hot) neighboring blocks or inactive (cool) neighbors – it can vary significantly between the hottest and coolest temperatures in as little as 0.2μm, making accurate thermal modeling critical.
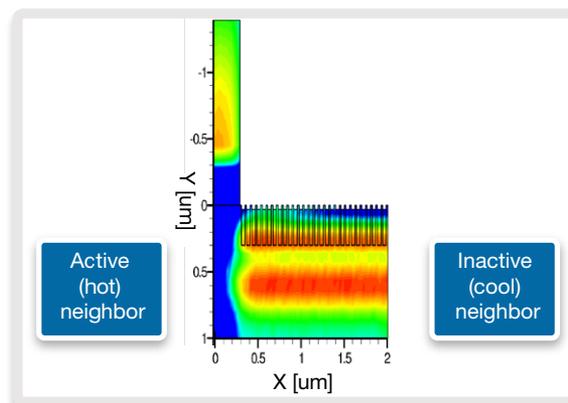

Figure 2. Thermal profile of the fins of a matched-pair across a temperature gradient

EDA Tools Readiness for 7nm Processes

The EDA ecosystem (Figure 3) has supported FinFET design since the inception of FinFET designs, and it continues to work for 7nm.
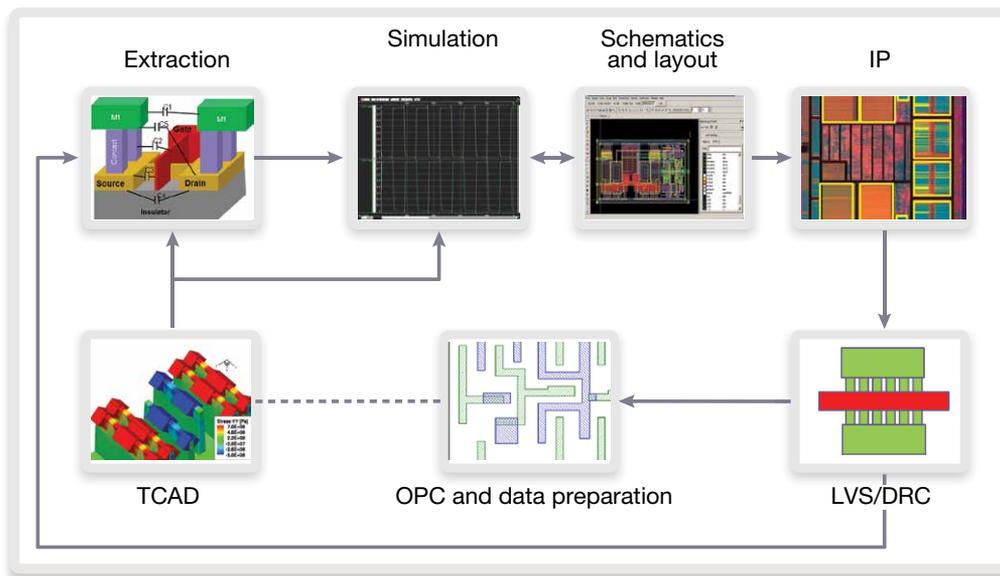

Figure 3. EDA ecosystem

The technology computer aided design (TCAD) part of the ecosystem includes elaborate and extensive front-end 3D simulation and modeling of the FinFET device behavior. The high aspect ratio etching/deposition (topography) of FinFETs requires additional process modeling analysis. Traditionally, in TCAD, these process geometries have not been modeled — they have been approximated geometrically. With the higher aspect ratio etching/deposition steps that advanced technologies bring, more designers are interested in physical simulation of the topography. 2D process modeling can be used for the fin generation process, but to really capture more complex behavior and proximity effects, 3D simulation is needed. This is especially true in the use of TCAD tools when optimizing SRAM bit-cells layout and connectivity where, in most cases, each transistor in the 6T bitcell is a single fin.

Device modeling and device simulation needs to capture effects of new surface orientation, surface scattering effects, quasi-ballistic transport, and corner effects. Mobility models need to adapted and recalibrated.

TCAD tools must deliver accurate 3D modeling of the FinFET device that addresses layout proximity effects, topology and architecture stress dependencies as well as electromigration. The tools should have direct links to Synopsys StarRC extraction and to the BSIM spice modeling arm of the simulators.

The BSIM-CMG (common multi-gate) model that is able to model FinFETs (double-gate, multi-gate) as well as gate all around (GAA) transistors with the channel completely surrounded by the gate, as in nanowires or pillar transistors, will be used for 7nm.

The FinFET parasitics device model is complex. Designers require efficient and accurate extraction techniques to handle the increasingly complex parasitics associated with the FinFET based circuits. A typical FinFET parasitics device model for a single FinFET is shown in Figure 4.
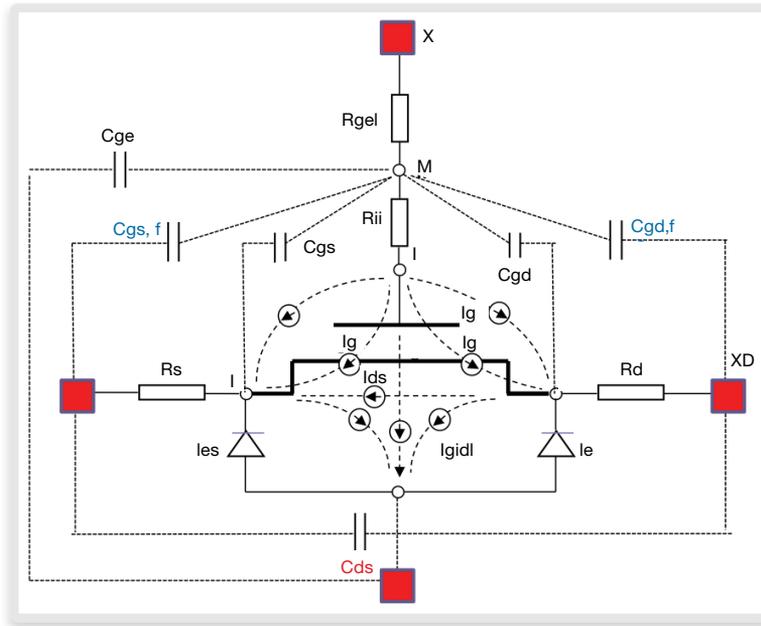
Figure 4. FinFET parasitics model

Figure 5A shows the middle of line (MOL) and back end of line (BEOL) of the 7nm 2-NAND library cell cited earlier. Figure 5B shows the detailed extracted parasitic capacitances for a particular realization scheme with four FinFETs. The parasitics model is very complex and designers need efficient methods to extract those parasitics in an acceptable time, such as with the Synopsys StarRC™ tool.
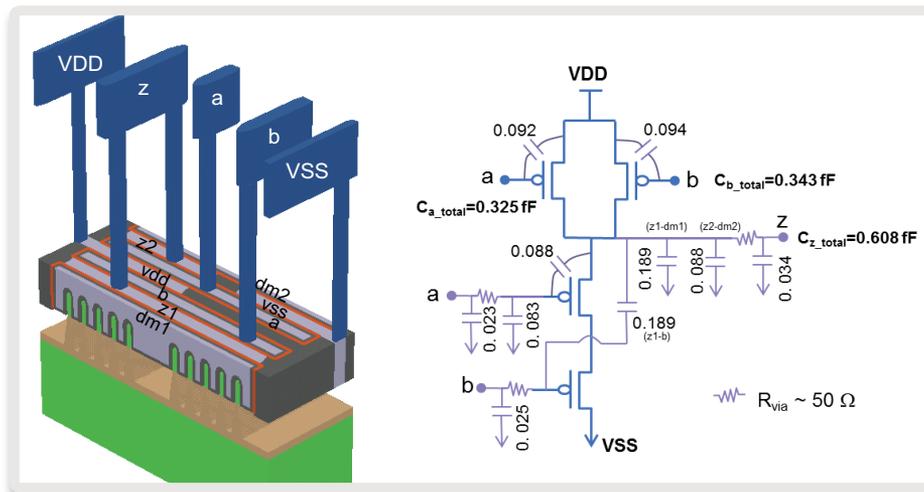

Figure 5. (A) MOL and BEOL of 2-input NAND (B) extracted parasitics model

Summary

The 7nm node is shaping up to be a very exciting yet challenging node for designers. Even with the performance and area benefits that the node brings, designers must understand the significant technical challenges stemming from increasing variability associated with tighter pitches and more complex lithography steps. Design for variability and reliability considerations will require comprehensive modeling and analysis as well as advanced circuit techniques such as on chip sensing and compensation.

Synopsys is uniquely qualified to help designers take on the 7nm challenge through a combination of a vast experience in earlier FinFET nodes and a complete IP (including embedded memory, logic library, and memory test), design and EDA ecosystem. We have already begun enabling 7nm designs through our EDA and IP solutions.

For More Information

‣ DesignWare Embedded Memories and Logic Libraries
‣ FinFET: The Promises and the Challenges
‣ White paper: Design, Test & Repair Methodology for FinFET-based Memories