Lab Exercise #6

Objective

- Continue working on Lab #5 and complete it.

References

Xilinx documents on the class web page.
Pinout for the WWU FPGA3 digital logic board (found on the class webpage).

Design Flow

Refine, as needed, the block diagram created in HW#6
As needed, create or add additional detail to your timing documentation
Create state diagram(s) for state machine(s).

Then work on the VHDL description and debugging.
Make sure in your VHDL description that you put in comment lines that clearly identify the function of each "chunk" of description. There should be reasonable correlation between your block diagram and sections of VHDL description. Recall that the VHDL describes hardware. Also, on sections of VHDL or circuit that you obtain from others the author must be clearly noted.

Possible help

If you don't have a functional DAC driver circuit you may use a driver circuit posted on the class web page with this Lab 6 definition.

Suggestion to aid debugging

Because you cannot connect a scope probe onto circuit nodes inside an FPGA, bring out signals that would be useful for debugging using the ExtOut or Tek signal lines where a scope or logic analyzer can be connected. If signals change slowly enough connect signals to LEDs to observe them. Monitor the analog output with the scope.

To Turn In

Follow the lab 5 instructions.