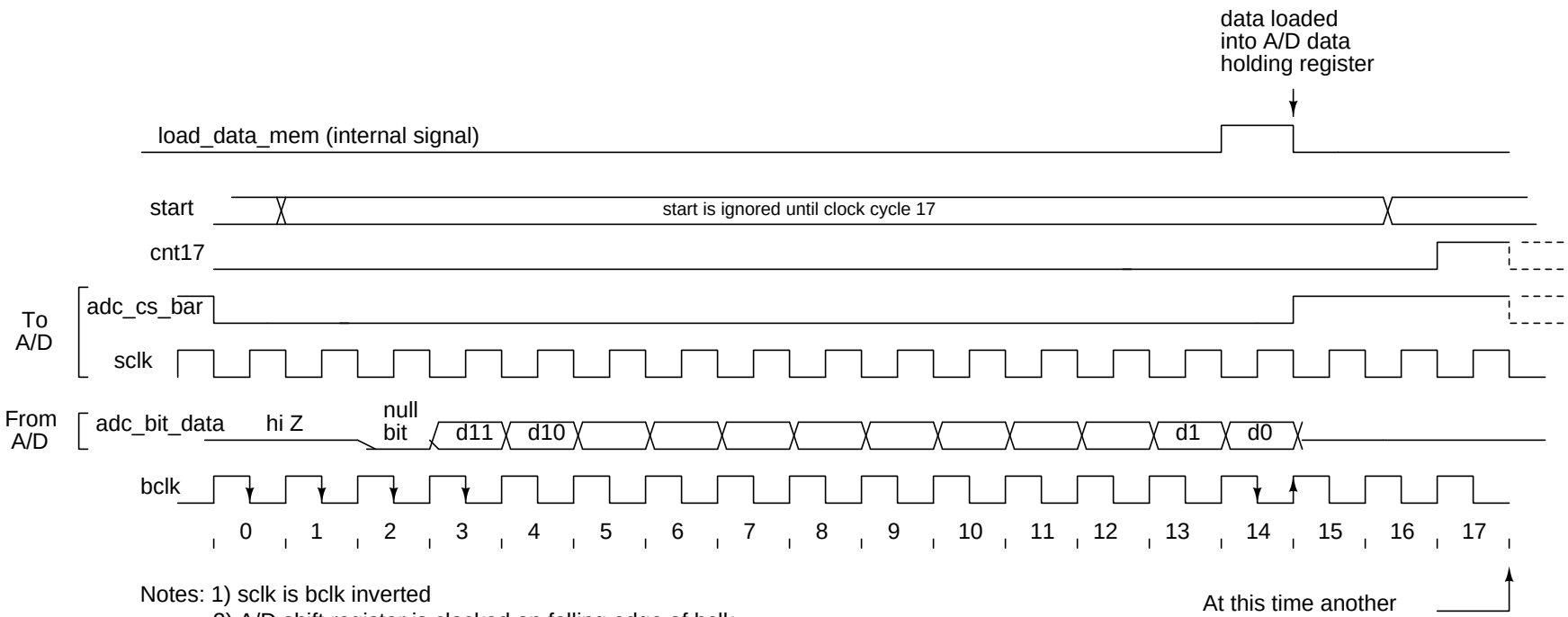

Notes: 1) sclk is bclk inverted
2) A/D shift register is clocked on falling edge of bclk
3) data is captured in the shift register on falling edge of bclk
4) cnt17 indicates when the 18th clock cycle occurs and may be useful to synchronize the ADC with other parts of the system
5) cnt17 may last for more than one clock cycle. It is asserted while adc state machine is in a holding state. If start is asserted while in this state then adc_cs_bar will be asserted and a new conversion sequence initiated at the next bclk rising edge.

At this time another A/D conversion can be initiated by lowering cs_bar.

Or there can be additional clock cycle(s) until cs_bar is asserted. It depends on if start is asserted or when it is asserted.

Driver inputs	Driver outputs
start	adc_data_word
bclk	adc_cs_bar
adc_bit_data	cnt17

Timing sequence driving a Microchip MCP3201 ADC

WWU PMOD A/D - D/A Board		
adc_interface_logic.vhd timing diagram		
L.Aamodt		5/23/21