Asynchronous Microprocessors

A Brief Overview
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"Delays have dangerous ends."
-William Shakespeare
Definitions

• Fully Asynchronous

• GALS (Globally Asynchronous Locally Synchronous)
Benefits

- No clock skew
- Adaptive & versatile
- Average-case instead of worst-case performance
- Low power requirements
- Reduced electrical noise
- Component modularity
- “Self Checking”

Figure 5: Amulet2e vs ARM7 EMC
Downsides

- Requires more transistor space
- No standard design methodology yet
- Not as many design tools (this is changing)
- Very few people trained in the design methods
- Logic synthesis is more complex
Asynchronous Basics

- Perform synchronization without a global clock
- Delay insensitive versus quasi-delay insensitive circuits (DI vs. QDI)
- Arbiters
- Isochronic forks?
Some Delay Knowledge Needed

- Delay insensitive logic is restrictive
- In order to have Turing Complete logic, some delay must be taken into account (i.e. QDI)
- An isochronic fork (right)
ILLIAC II (1958)

- Asynchronous logic design (100 times faster than competing machines of the time)
- Used Speed Independent Circuitry (no clock)
- One of the first pipelined computers
Caltech Asynchronous Microprocessor (CAM, 1988)

- 16-bit RISC, 2-micron CMOS
- Created their own set of design tools and languages to aid design (CHP, HSE, PRS)
- First asynchronous microprocessor
- Fully functional on first silicon
- 26 MIPS, 100 mA at 10V
- Able to run on a potato (300KHz at 0.9V)
Asynchronous MIPS R3000 (1998)

- 32-bit RISC ISA, 1.5 million transistors
- First asynchronous processor that was competitive with synchronous designs
- 190 MIPS @ 4W @ 3.3V @ 25°C
- 1V (9.66MHz @ 0.021 W) to 8V
- Functional on first silicon
- Operated at 180 MHz
- Compare to MIPS R3000, which operated at around 47MHz
**AMULET3 (2000)**

- 0.35 µm processor
- Ran at over 100 MIPS – the same as a contemporary ARM9
- Compatible with ARM level 4 instruction set
- Almost went to market in the DRACO commercial prototype (kept from doing so due to financial difficulties)
Future considerations

- Industry is slow to adopt asynchronous design practices, despite obvious benefits
- Anything modeling biological systems needs some level of asynchronous design
- GALS may be the intermediary to totally asynchronous designs (2009 SpiNNaker chip shown right)
- SpiNNaker project goal is to eventually include 50,000 chips to model neural network
Sources

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