Computer Organization and Design: The Hardware/Software Interface
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Errata list as of 9/01/14

Chapter		Page #	Description	Correction
Preface		xviii	On page xviii, 9th line, the text says "Appendix C on logic design..."	The Basics of Logic Design has been moved to **Appendix B**.
Preface		xviii	On page xviii, 14th line, the text says "this firth edition"	Should read "this **fifth** edition"
Preface		xix	On page xix, the first subheading says "Changes for the Fifth Edition"	Subheading should read "**Instructor Support**"
1		10		
1		12	In the "Peformance via Prediction" section, the first sentence incorrectly states that "the final great idea is prediction."	The sentence should read: "…the next great idea is prediction."
1		40	On page 40, the 2nd line of the caption for FIGURE 1.16, refers to "25 years"	Caption should say "**30** years" to be consistent with statement in the first sentence of Section 1.7.
1		55	Exercise 1.6 asks "which implementation is faster?"	For clarity, replace "which implementation is faster?" with "**Which is faster: P1 or P2?**"
1		58	Exercise 1.12.4 states: "Assume that 40% of the instructions executed on both P1 and P2 are floating-point instructions. Find the MFLOPS figures for the **programs**."	P1 and P2 are processors. Therefore, "programs" should read "**processors**".
1		59	On page 59, third line from the bottom (in the "Answers to Check Yourself"), it reads" §1.6, page 33: 1. a: both, b: latency, c: neither. 7 seconds.	There are two sub-questions, 1 and 2, for this problem. Therefore there should be a "**2.**" preceding "7 seconds": §1.6, page 33: 1. a: both, b: latency, c: neither. **2.** 7 seconds.
1		59	On page 59, Question 1.14 reads: "Assume a program requires the execution of 50 × 106 FP instructions, 110 × 106 INT instructions, 80 × 106 L/S instructions, and 16 × 106 branch instructions."	The "6" in each string of "106" should be superscript: "Assume a program requires the execution of 50×10^6 FP instructions, 110×10^6 INT instructions, 80×10^6 L/S instructions, and 16×10^6 branch instructions."
2		128	In the "Answer" section of the "Linking Object Files" example, the paragraphs above and below the table are identical.	Second instance of the paragraph should be removed.
2		135	In the section "**The Procedure** `sort`" the code example: The inner for loop does `(j=i-1; j>=0 && v[j]>v[j+1]; j =1)`, though the latter should surely be `j+=1 (or j++, j = j+1)` - since otherwise the same comparison is made every time, for all `i` (the outer loop), so it may as well execute once. I'd suggest having made that change, that it's more readable to check `v[j] > v[i]`, since `j` is defined `i-1`, odd to then use `i-1+1`.	[Needs confirmation]

2	164	Exercise 2.2: Problem statement reads "For the following MIPS assembly instructions above…"	The problem statement should read "For the following MIPS assembly instructions **below**…"
2	165	Exercise 2.5: Problem statement reads "For the MIPS assembly instructions in Exercise 2.4, rewrite the assembly code to minimize the number if MIPS instructions..."	The problem statement should read "For the MIPS assembly instructions in Exercise 2.4, rewrite the assembly code to minimize the number **of** MIPS instructions..."
2	168	Exercises 2.18.1 and 2.18.2: Problem statement reads "How this would this affect the size of …"	The problem statement should read "How **would this** affect the size of …"
2	171	Exercise 2.31: At the end of the code the closing parentheses "}" is missing.	There should be one more line that has only "}", with it leftmost aligned. Similar to code in Question 2.34
2	171	Exercise 2.34: Relative time rating and reference section are missing.	Relative time and reference section should read: 2.34 **[5] <$2.8>**
2	172	Exercise 2.37, 8th line reads: "50ten, 52ten, 0ten"	The 8th line should read ("ten" in subscript): 50_{ten}, 52_{ten}, 0_{ten}
2	173	Exercise 2.42 reads "If the current value of the PC is `0x1FFFf000`, ..." The value string "F" and "f" are mixed.	All the F's should be capital, ie: "**0x1FFFF000**"

	Page	Description	Correction
3	206	On page 206, the 4th line reads: "Since 127 >= +4 >= -126, there is no overflow or underflow."	The "+4" should be "-4", since the exponent of the final result above is "-4". Therefore the line should read: "Since 127 >= **-4** >= -126, there is no overflow or underflow."
3	223	Figure 3.19, the 4th and 5th lines, in the "Data transfer" column, read: "VLD(1,2,3.4)" and "VST(1,2,3.4)" The punctuation between "3" and "4" is a period (.)	The 4th and 5th lines should read: VLD(1,2,3,4) and VST(1,2,3,4)
3	225	The 8th line reads "instruction to perform two 64-bit floating-point multiplies." However, the 9th and 11th lines show these instructions: "`addpd`" and "`vaddpd`" Therefore, the text and the example instructions do not correspond.	The 8th line should read: "instruction to perform two 64-bit floating-point **additions**"
3	225	Elaboration section, 3rd line reads: `vaddpd %ymm0, %ymm1, %ymm4  #  %ymm4 = %ymm1 + %ymm2` The variable names in the comment portion do not correspond to those in the real expression part.	Comment portion should read: `#  %ymm4 = %ymm0 + %ymm1`
3	226	Figure 3.21 caption reads: "Unoptimized C version..." Figure 3.22 caption reads: "...the optimized C code in Figure 3.21"	Figure 3.22 caption should read: "...the **unoptimized** C code in Figure 3.21"
3	226	Figure 3.22, 11th line reads: `11. add   $0x1, %r11d     # register %r11 = %r11 + 1`	In the 11th line, "`%r11d`" should be "**`%r11`**": `11. add   $0x1, %r11     # register %r11 = %r11 + 1`
	229	On page 229, 6th line reads: "Recall that a binary number c, where x_i means the ith bit, represents the number"	The 6th line should read: ""Recall that a binary number x, where x_i means the ith bit, represents the number"

3		229	The first equation reads: … + $(x^3 \times 2^3) + (x^2 \times 2^2)$ 1 $(x1 \times 2^1) + (x0 \times 2^0)$	The first equation should read: … + $(x3 \times 2^3) + (x2 \times 2^2) + (x1 \times 2^1) + (x0 \times 2^0)$
3		229	The 8th line reads: "Shifting the bits of c right by n bits would seem to be the same as dividing by…"	The 8th line should read: "Shifting the bits of x right by n bits would seem to be the same as dividing by…"
3		229	The 9th line reads: "$2n$ …"	The 9th line should read: "2^n …"
3		240	Exercises 3.35, 3.36, 3.37 read "… $(3.41796875 \ 10^{-3} \ … \ )$"	Exercises 3.35, 3.36, 3.37 should read "… $(3.41796875 \times 10^{-3} \ … \ )$"
3		241	Exercises 3.43, 3.44, 3.45, 3.46. In Exercise 3.43, "value 1/3" is indicated. In the other exercises, it is not.	In exercises 3.45 and 3.46 should be re-worded to include "the fraction 1/3"
3		241	Exercise 3.47, 6th line (just below the equation) reads: "Assume you are to write an optimized implementation this code …"	Exercise 3.47, 6th line (just below the equation) should read: "Assume you are to write an optimized implementation of this code …"
4		277	On page 277, the 7th line from the bottom (a sub-heading) reads: **Hazards**	The sub-heading should read: **Structural Hazards**

4	282	On page 282, the 1st sentence of the ANSWER section reads: "Figure 3.27 in Chapter 3 shows that branches are 17% of the instructions executed in SPECint2006."	The 1st sentence of the ANSWER section should read: "Figure 3.28 in Chapter 3 shows that branches are 17% of the instructions executed in SPECint2006."
4	286	On page 286, last paragraph of Section 4.5 is: "Instruction sets can either simplify or make life harder for pipeline designers, who must already cope with structural, control, and data hazards. Branch prediction and forwarding help make a computer fast while still getting the right answers."	The last paragraph of Section 4.5 should be included in the "BIG Picture" section that appears directly above it.
4	291	Figure 4.36, upper left, the "PC" box is not highlighted.	The "PC" box should be highlighted, since it is active.
4	291	In Figures 4.36, 4.38, and 4.40, there are two copies of the data path in each figure. In the top copy, the MUX after the MEM/WB pipelined registers has its 0,1 inputs swapped; in the bottom copy of the data path, the 0,1 inputs to this MUX are correct.	In the top data path, the MUX after the MEM/WB pipelined registers should read **1,0**.
4	328	On page 328, 4 lines above EXAMPLE, reads: "In reality, we save the address +4, so the exception handling the software routine must first subtract 4 from the saved value."	The sentence should read (delete "the software"): "In reality, we save the address +4, so the exception handling routine must first subtract 4 from the saved value."
4	338	On page 338, the definition in the upper left margin reads: "**loop unrolling** A technique to get more performance from loops that access arrays, in which multiple copies of the loop body are made and instructions from different iterations are"	The definition should read ("scheduled together" is missing from the conclusion of the sentence): "**loop unrolling** A technique to get more performance from loops that access arrays, in which multiple copies of the loop body are made and instructions from different iterations are **scheduled together**."
4	344	Figure 4.73 states that the Intel Core i5 Nehalem has "1" Cores/Chip.	The Cores/Chip for the Core i5 Nehalem should read "**2-4**"
4	348	On page 348, Figure 4.77, bottom right corner of figure, in the rectangle 1 line up from bottom right, reads: "256 KB unified l2 cache (eight-way)"	The text should read ("L2" instead of "l2"): "256 KB unified **L2** cache (eight-way)"
4	351	On page 351, 6 and 5th lines from bottom, reads: "We surround each intrinsic with a simple for loop that 4 iterations (lines 9, 14, and 20) ..."	The 6 and 5th lines from bottom should read ("loop with" rather than "loop that"): "We surround each intrinsic with a simple for loop **with** 4 iterations (lines 9, 14, and 20) ..."
4	353	On page 352, 9 to 7th lines from bottom, read: "Optimizations for subword parallelism and instruction level parallelism result in an overall speedup of 8.8 versus the unoptimized DGEMM in Figure 3.21."	In Figure 4.82, the GFLOPS values for unoptimized and AVX+unroll are 1.7 and 14.6, respectively. The speedup rate between them is therefore about 8.59. The sentence should read: "Optimizations for subword parallelism and instruction level parallelism result in an overall speedup of **8.59** versus the unoptimized DGEMM in Figure 3.21."

4	353	On page 353, Figure 4.81 shows:
		
		`9 vmulpd (%rax),%ymm0,%ymm5       # Parallel mul %ymm1,4 A`
		
		`...`
		
		`11 vmulpd 0x20(%rax),%ymm0,%ymm5    # Parallel mul %ymm1,4 A elements`
		
		`...`
		
		`13 vmulpd 0x40(%rax),%ymm0,%ymm5    # Parallel mul %ymm1,4 A elements`
		`14 vmulpd 0x60(%rax),%ymm0,%ymm0    # Parallel mul %ymm1,4 A elements`
		
		In these lines, the suffix number for the variable %ymm in the comment part differs from that in the command part.
			The comments for these 4 lines should read
			
			`# Parallel mul %ymm0,4 A elements`

4	353	On page 352, Figure 4.81 shows: `19 jne 68 <dgemm+0x68>       # jump if not %r8 != %rax`	"`not`" and "`!=`" are redundant. The line should read: `19 jne 68 <dgemm+0x68>       # jump if %r8 %rax`
4	369	On page 369, Question 4.19 reads: 4.19.1 [10] <§§4.3, 4.6, 4.14>	The reference section 4.14 in this question should read 4.15. The same applies to sub-questions that follow.
5	386	On page 386, lower part, in the table without Figure No.: In the "Hit or miss in cache" column, reference is made to (5.6b), (5.6c), and so on.	Figure 5.9 is the actual reference. Therefore (5.6b), (5.6c), etc. should be (5.9b), (5.9c), etc.
5	414	On page 414, Figure 5.20, Names of Arrays: In the body description, C, A, and B are used as the names of arrays. However, in this figure, x, y, or z appears above the top left corner of each square.	Array names should be: x to C, y to A, and z to B
5	414	On page 414, Figure 5.20, 3rd line of caption reads: Compared to Figure 5.21, elements ...	The 3rd line should read: Compared to **Figure 5.22**, elements ...
5	414	On page 414, Figure 5.20, last line of caption reads: … new elements of x.	The last line of the caption should read: … new elements of **C**.

5		414	On page 415, Figure 5.22, Names of Arrays In the body description, C, A, and B are used as the names of arrays. However, in this figure, x, y, or z appears above the top left corner of each square.	Array names should be: x to C, y to A, and z to B
5		422	On page 422, 2nd line from end of ANSWER reads: Parity bits 2 and 10 are incorrect.	In the EXAMPLE description, parity bit 8 is said to have an error. Therefore, "10" should be "8". The text should read: "Parity bits 2 and **8** are incorrect"
5		462	On page 462, 4th line reads: 32-byte addresses	The 4th line should read: "32-**bit** addresses".
5		472	On page 472, Figure 5.44, heading of right most column, reads: Intel Nehalem	The heading of right most column should read: Intel Core i7
5		489	Page 489, Question 5.9.3 The relative time rating and the reference section are missing.	The relative time rating and the reference section are the same as questions 5.9.1 and 5.9.2, ie: [5] <5.5>

6		533	On page 533, 5th line in the code in the "Hardware/Software Interface" reads:
			
			`EmitIntermediate(w, "1"); // Produce list of all words reduce(String key, Iterator values):`
				The 5th line in the code in the "Hardware/Software Interface" should read (line break inserted after "words"):
				
				`EmitIntermediate(w, "1"); // Produce list of all words`
				`reduce(String key, Iterator values):`

6		533	On page 533, 2nd line from bottom in the "Hardware/Software Interface" reads:
			
			`result += ParseInt(v); // get integer from key-value pair`
				In the first paragraph on the next page, `ParseInt()` is explained to get the number of occurrences per word in all documents. To avoid confusion, change "integer" to this descriptive expression:
				
				`result += ParseInt(v); // get integer value from key-value pair`
				`// value represents number of occurrences per word in all documents`

6	538	4. Page 538, 4th line in the caption of Figure 6.14 reads: an n-dimensional interconnect with 2n nodes,	The "n" in "with 2n" should be superscript: an n-dimensional interconnect with 2^n nodes,
6	551	On page 551, Figure 6.22, last row reads: Peal double-precision SIMD FLOPS (GFLOP/sec)	"Peal" should read "Peak"
6	552	On page 552, Figure 6.23, the 4th - 3rd lines from bottom of the caption reads: ... and 78 DP GFLOP/sec and 512 DP GFLOP/sec on the GTX 280.	The caption text should be changed so that "512 DP GFLOP/sec" reads "624 SP GFLOP/sec": ... and 78 DP GFLOP/sec and **624 SP GFLOP/sec** on the GTX 280.
6	554	On page 554, 2nd paragraph, 3rd line reads: "accesses are to data are aligned on 16-byte boundaries."	The 3rd line should read: "accesses to data are aligned on 16-byte boundaries"
6	555	On page 555, 14th line from bottom reads: "DGEMM operates now operates at 174 GLOPS for 960 × 960 ..."	The 14th line from the bottom should read: "DGEMM now operates at 174 GFLOPS ..."
6	555	On page 555, 12th line from bottom reads: "… just 0.8 GFOPS, …"	The 12th line from bottom should read: "… just 0.8 **GFLOPS**, …"
6	570	On page 569, Question 6.9, 5th line reads CPU SMT: This is not used in the following sub questions.	Add this question: "6.9.4 [10]<6.4> Assume you have 1 SMT CPU. How any cycles will it take to execute the two threads? How many issue slots are wasted due to hazards?"
6	572	On page 572, Question 6.18, 5th line reads: "One the earliest sparse matrix representations is the Yale Sparse Matrix Format."	The 5th line should read: "One **of** the earliest sparse matrix representations is the Yale Sparse Matrix Format."
App A		On page A50, Figure A.10.2 the file of values on the left side of the rightmost column are missing.	In Figure A.10.2, the file of values on the left side of the rightmost column should be 0-63 (same as the other columns).

Notes