Digital Logic Homework #12

DUE: Friday, November 8

Objective

To design various state machines using rising-edge-triggered (RET) D flip-flops.

To Do - Design

1. Design a two-bit grey-code counter with an up/down switch. When the switch is asserted the state machine should count up, otherwise it should count down.

2. Design a state machine that implements the following sequence and repeats indefinately:

   $00 \rightarrow 10 \rightarrow 00 \rightarrow 11$

To Do - Implementation

1. Wire up one of the two circuits above;
2. Bring your circuit to class on the due date and demonstrate it;
3. Use a switch as the clock or the 1Hz signal provided on your logic boards;
4. Be sure and tie the asynchronous *preset* and *clear* inputs high on both D flip-flops.

Turn In

- **Staple this assignment sheet** to your paper design, which is to be done in accordance with the school of engineering homework guidelines posted on the course web page.
- Notes and results on circuit construction, debugging, and operation.