Engr354: Digital Logic

Chapter 1: Design Concepts

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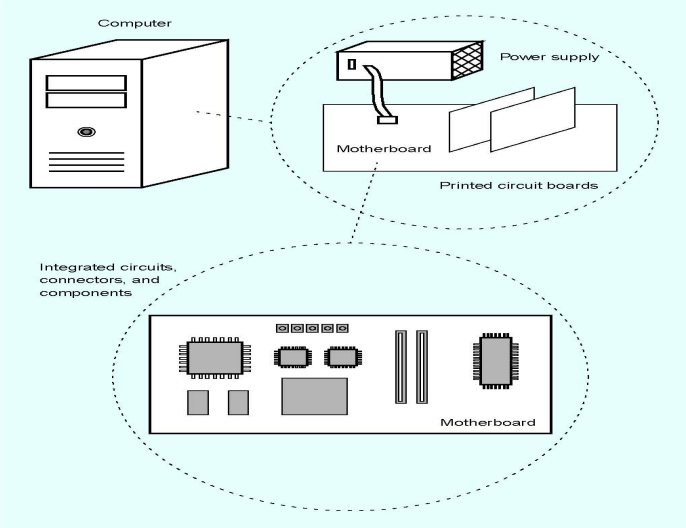
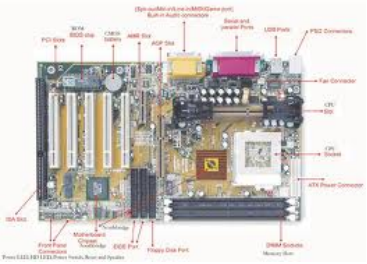
Presentation Overview

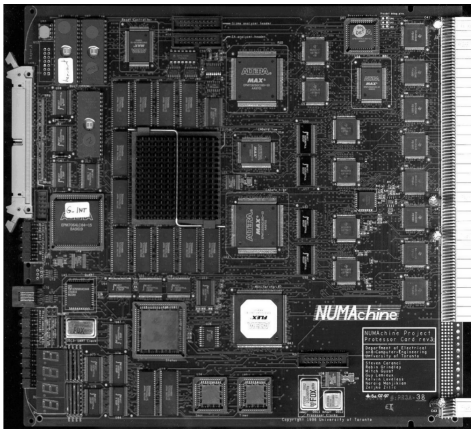
- Digital hardware systems;
- Digital hardware implementation methods;
  - Standard chips;
  - Programmable logic devices (PLD's);
  - Application Specific Integrated Circuits (ASIC's);
  - Fully custom IC's;
  - VHDL.
- Design process.

A Digital Hardware System

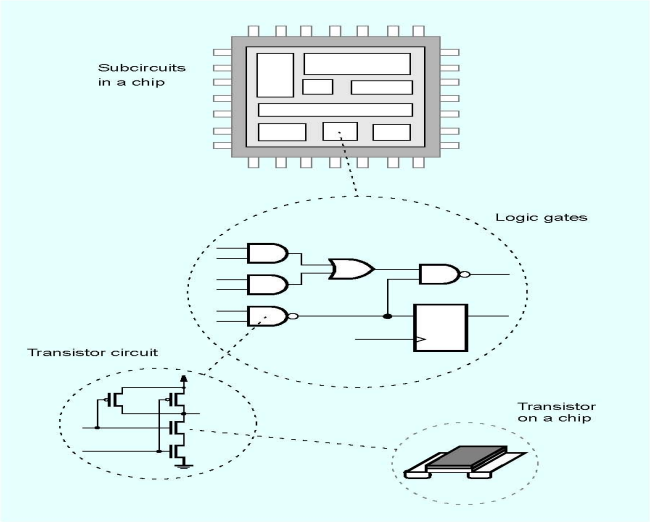


Printed Circuit Boards

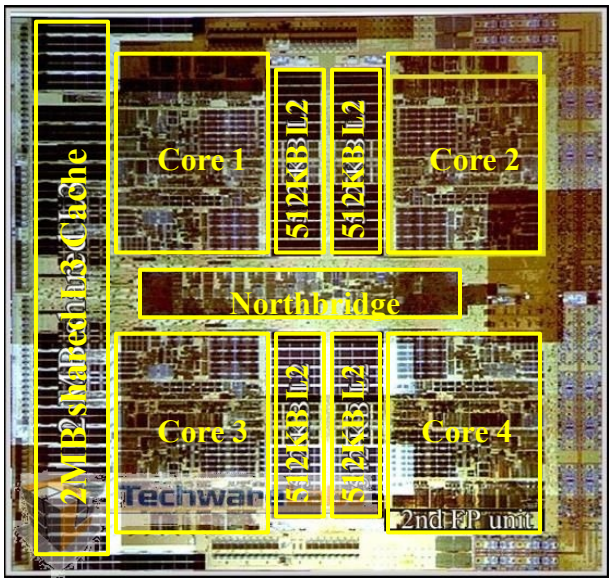




Design Abstraction

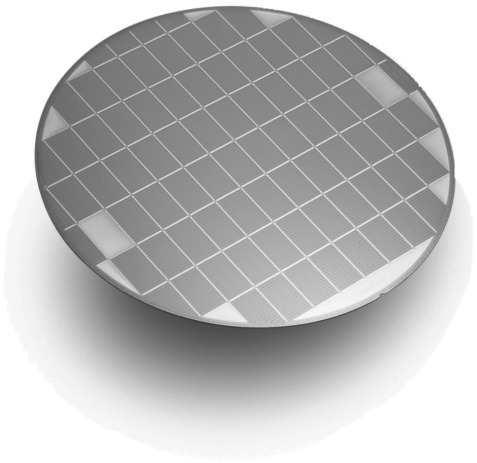


AMD's Barcelona Multicore Chip



- Four out-of-order cores on one chip
- 1.9 GHz clock rate
- 65nm technology
- Three levels of caches

A Silicon Wafer



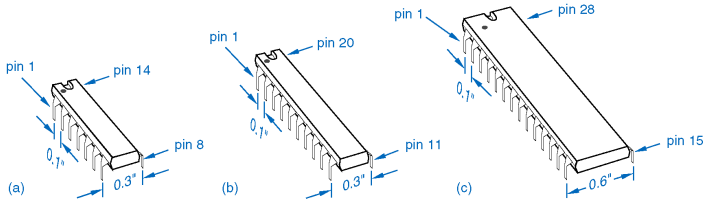
ITRS Roadmap

Table 1.1 A sample of the International Technology Roadmap for Semiconductors.

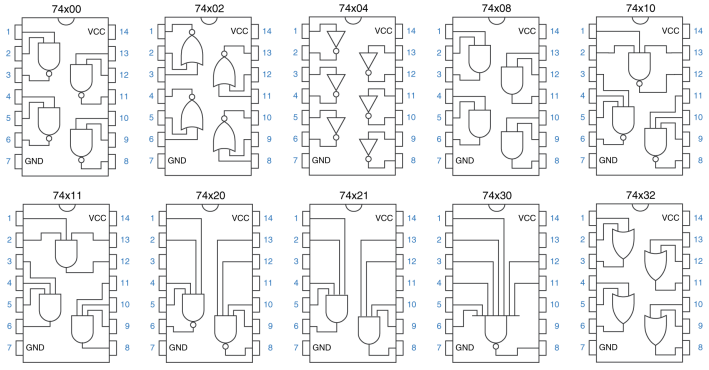
	Year					
	2006	2007	2008	2009	2010	2012
Technology feature size	78 nm	68 nm	59 nm	52 nm	45 nm	36 nm
Transistors per cm^2	283 M	357 M	449 M	566 M	714 M	1,133 M
Transistors per chip	2,430 M	3,061 M	3,857 M	4,859 M	6,122 M	9,718 M

Standard Chips

- Realize common logic functions;
- Usually less than 100 transistors;
- Common ones will be found in your lab kits;
- You will use them in some homework assignments;
- Not used much today as they occupy too much space on printed circuit boards (PCB's).



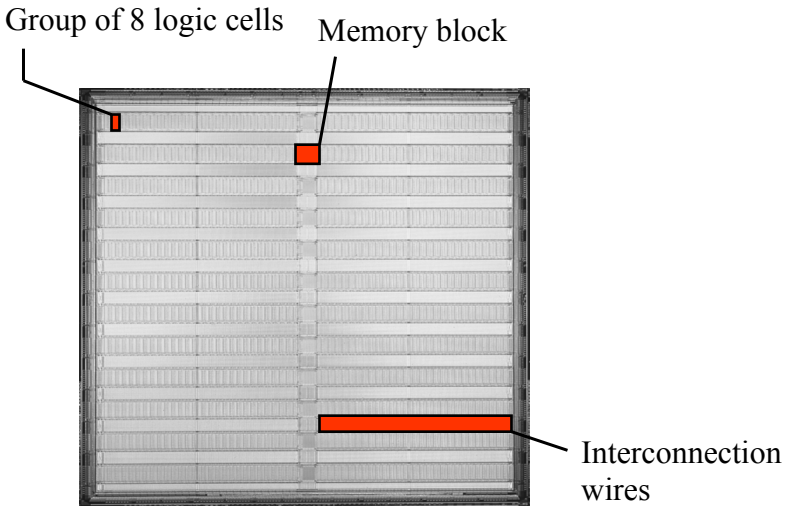
Standard Chips



Programmable Logic Devices (PLD's)

- Realize much more complicated logic circuits than a standard chip;
- Often reprogrammable;
- Field-programmable gate arrays (FPGA) will soon use more than 100 million transistors;
- Widely used today.

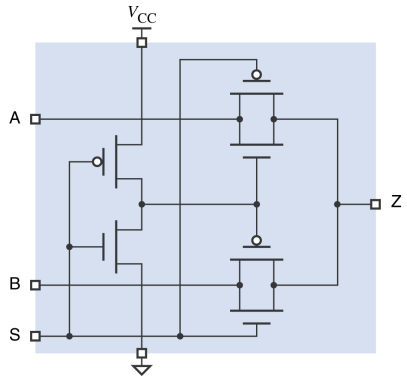
Field Programmable Gate Array (FPGA)



Custom Designed Chips

- PLD's are not very efficient so they may not meet performance or cost objectives;
- May need to design a *custom* or *semi-custom chip* (ASIC);
- Advantage - optimized for a given task;
- Disadvantage: more complex design and manufacturing process, more design time;
- Fluke microprocessor example.

Custom Designed Chips



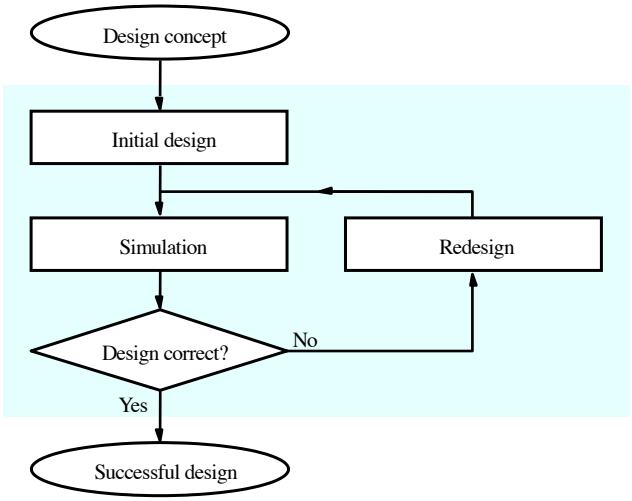
VHDL – A Structured Programming Language

```
library IEEE;
use IEEE.std_logic_1164.all;

entity Vchap1mux is
    port ( A, B, S: in  STD_LOGIC;
           Z:       out STD_LOGIC );
end Vchap1mux;

architecture Vchap1mux_arch of Vchap1mux is
begin
  Z <= A when S = '0' else B;
end Vchap1mux_arch;
```

Basic Digital Design Loop



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