Engr354: Digital Logic Circuits

Chapter 7
Sequential Logic Elements

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Sequential Logic Elements

In this chapter you will learn about

- Logic circuits that can store information;
- Basic cells, latches, and flip-flops;
- State diagrams;
- Design techniques for circuits that use flip-flops.

Circuit Types

- ***Combinational*** – output depends only on the input.
- ***Sequential*** – output depends on input and past behavior
  - Requires use of storage elements;
  - Contents of the storage elements is called *state;*
  - Circuit goes through a sequence of states as a result of changes in inputs.
- ***Synchronous*** – controlled by a clock.

Clock Signals

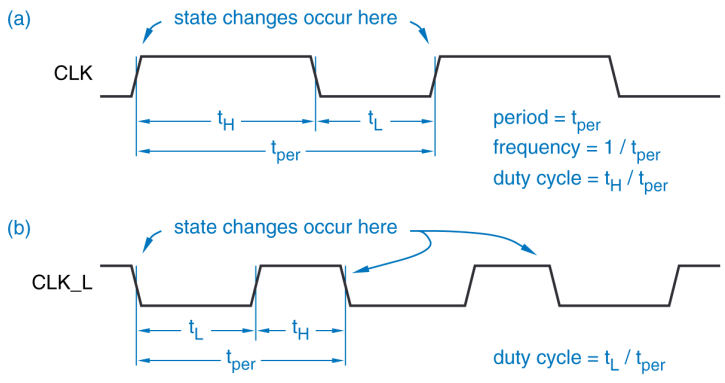
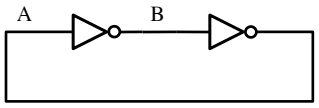


Figure 7-1

Clock signals: (a) active high; (b) active low.

A Bistable Memory Element

- Bistable – possessing two stable states.



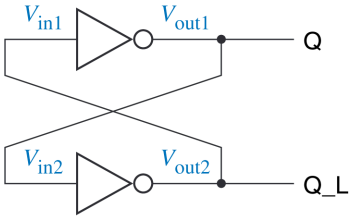
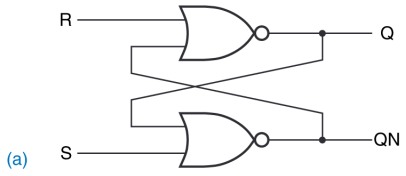


Figure 7-2
A pair of inverters forming a bistable element.

A Set/Reset (SR) Memory Element

- Called a ***Basic Cell;***
- NOR centered Basic Cell:
  - Circuit (a), Function table (b).
- Inputs are active when they are ***high;***
- Blocking side inputs.



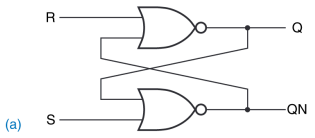
(a)

(b)

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

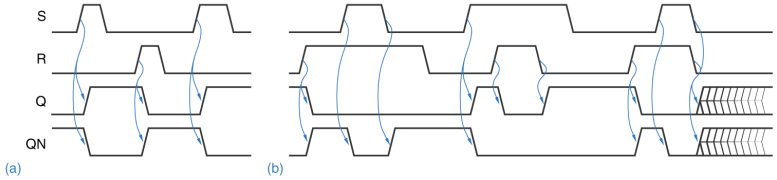
Typical Operation of a *Basic Cell*

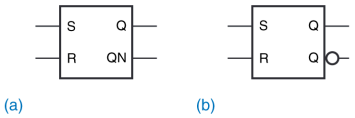
- Reset, clear.
- Set, preset.



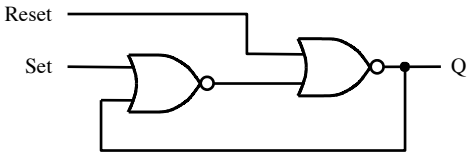
S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

(b)





NOR-Centered (Reset Dominant) Basic Cell



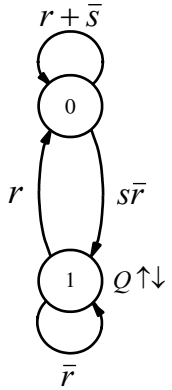
Circuit

S	R	Action	Q_{n+1}
0	0	hold	Q_n
0	1	reset	0
1	0	set	1
1	1	reset	0

Operation Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
	ϕ	1
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	ϕ	1
$1 \rightarrow 1$	ϕ	0

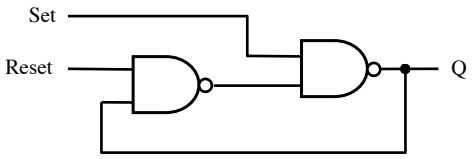
Excitation Table



State Diagram

NAND-Centered (Set Dominant) Basic Cell

- Inputs are active low (when they are ***asserted***);
- Operation table indicates assertion, not voltage, levels.



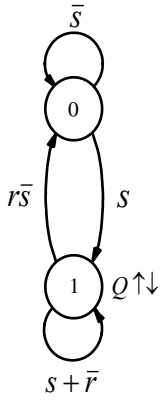
Circuit

S	R	Action	Q_{N+1}
0	0	hold	Q_N
0	1	reset	0
1	0	set	1
1	1	set	1

Operation Table

$Q_n \to Q_{n+1}$	Inputs S	R
$0 \to 0$	0	ϕ
$0 \to 1$	1	ϕ
$1 \to 0$	0	1
$1 \to 1$	1	ϕ
	ϕ	0

Excitation Table



State Diagram

Combined Form of the Basic Cell

$Q_n \to Q_{n+1}$	Inputs S	R
$0 \to 0$	0	ϕ
$0 \to 1$	1	ϕ
$1 \to 0$	0	1
$1 \to 1$	1	ϕ
	ϕ	0

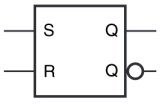
Excitation Table NAND-centered

$Q_n \to Q_{n+1}$	Inputs S	R
$0 \to 0$	0	ϕ
	ϕ	1
$0 \to 1$	1	0
$1 \to 0$	ϕ	1
$1 \to 1$	ϕ	0

Excitation Table NOR-centered

$Q_n \to Q_{n+1}$	Inputs S	R
$0 \to 0$	0	ϕ
$0 \to 1$	1	0
$1 \to 0$	0	1
$1 \to 1$	ϕ	0

Excitation Table Combined Form



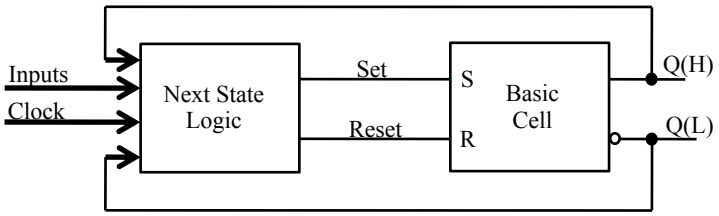
Basic Cell

Designing Latches - A Model

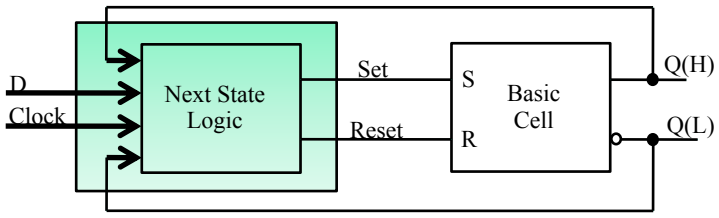
- Latch - a logic circuit that transfers the input state to the output state when the *clock* signal is high and latches and holds the input when the *clock* signal goes low.

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

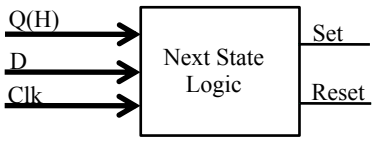
Excitation Table Combined Form



Design of a Clocked D (Data) Latch



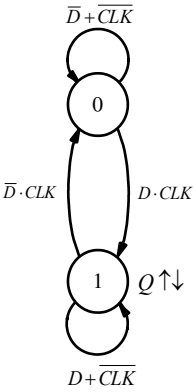
Design of a Clocked D Latch



Block Diagram

Clk	D	Qn	Qn+1	Set	Reset
0	0	0	0	0	ϕ
0	0	1	1	ϕ	0
0	1	0	0	0	ϕ
0	1	1	1	ϕ	0
1	0	0	0	0	ϕ
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	1	ϕ	0

Truth Table



State Diagram

Clk	D	Action	Q_{N+1}
0	x	hold	Q_N
1	0	reset	0
1	1	set	1

Operation Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

Excitation Table
Basic Cell

$$Set = clk \cdot D$$
$$Reset = clk \cdot \overline{D}$$

Equations

Clocked D Latch

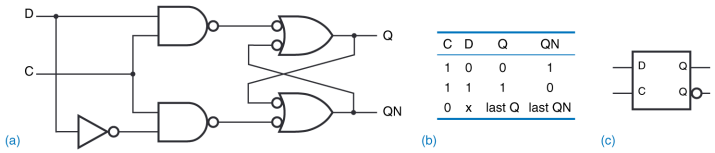


Figure 7-12
D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

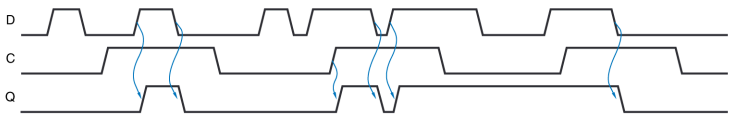
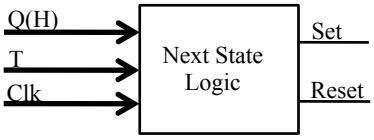


Figure 7-13
Functional behavior of a D latch for various inputs.

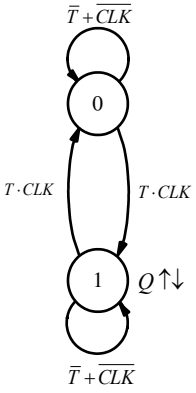
Design of a Clocked Toggle (T) Latch



Block Diagram

Clk	T	Qn	Qn+1	Set	Reset
0	0	0	0	0	ϕ
0	0	1	1	ϕ	0
0	1	0	0	0	ϕ
0	1	1	1	ϕ	0
1	0	0	0	0	ϕ
1	0	1	1	ϕ	0
1	1	0	1	1	0
1	1	1	0	0	1

Truth Table



State Diagram

Clk	T	Action	Q_{N+1}
0	x	Hold	Q_N
1	0	Hold	Q_N
1	1	Toggle	$\overline{Q}_N$

Function Table

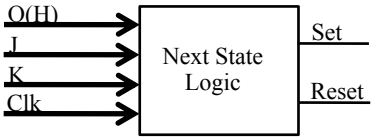
$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

Excitation Table Basic Cell

$$Set = clk \cdot T \cdot \overline{Q}$$
$$Reset = clk \cdot T \cdot Q$$

Equations

Design of a Clocked JK Latch



Block Diagram

Clk	J	K	Qn	Qn+1	Set	Reset
0	0	0	0	0	0	ϕ
0	0	0	1	1	ϕ	0
0	0	1	0	0	0	ϕ
0	0	1	1	1	ϕ	0
0	1	0	0	0	0	ϕ
0	1	0	1	1	ϕ	0
0	1	1	0	0	0	ϕ
0	1	1	1	1	ϕ	0
1	0	0	0	0	0	ϕ
1	0	0	1	1	ϕ	0
1	0	1	0	0	0	ϕ
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	0	1	1	ϕ	0
1	1	1	0	1	1	0
1	1	1	1	0	0	1

Truth Table

Clk	J	K	Action	Q_{N+1}
0	x	x	Hold	Q_N
1	0	0	Hold	Q_N
1	0	1	Reset	0
1	1	0	Set	1
1	1	1	Toggle	$\overline{Q}_N$

Function Table

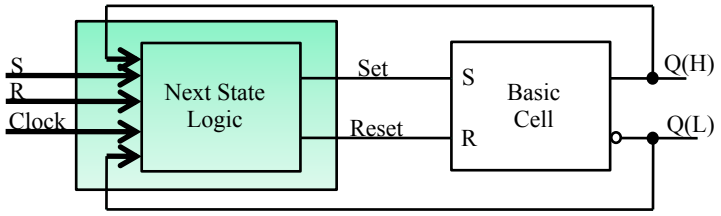
$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

Excitation Table Basic Cell

$$Set = clk \cdot J \cdot \overline{Q}$$
$$Reset = clk \cdot K \cdot Q$$

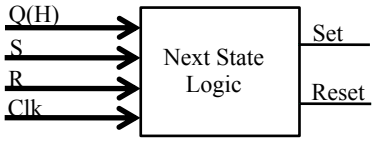
Equations

Design of a Set-Dominant Clocked SR Latch



- Inputs – S, R, Clock, Q
- Outputs – Set, Reset

Design of a Set-Dominant Clocked SR Latch



Block Diagram

S	R	Action	Q_{N+1}
0	0	hold	Q_N
0	1	reset	0
1	0	set	1
1	1	set	1

Operation Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

Excitation Table Basic Cell

$$Set = clk \cdot S$$

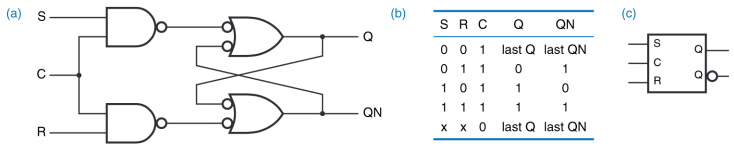
$$Reset = clk \cdot R \cdot \overline{S}$$

Equations

Clk	S	R	Qn	Qn+1	Set	Reset
0	0	0	0	0	0	ϕ
0	0	0	1	1	ϕ	0
0	0	1	0	0	0	ϕ
0	0	1	1	1	ϕ	0
0	1	0	0	0	0	ϕ
0	1	0	1	1	ϕ	0
0	1	1	0	0	0	ϕ
0	1	1	1	1	ϕ	0
1	0	0	0	0	0	ϕ
1	0	0	1	1	ϕ	0
1	0	1	0	0	0	ϕ
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	0	1	1	ϕ	0
1	1	1	0	1	1	0
1	1	1	1	1	ϕ	0

Truth Table

SR Latch with Enable (Clock)



S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

Figure 7-10

S-R latch with enable: (a) circuit using NAND gates; (b) function table; (c) logic symbol.

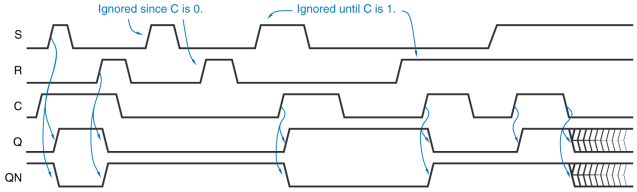
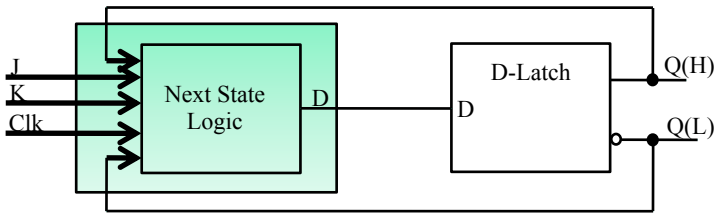


Figure 7-11

Typical operation of an S-R latch with enable.

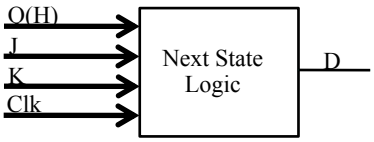
Design of a Clocked JK Latch – Version II

- Replace the basic cell with a D-latch as the memory element.



- Inputs – J, K, Clk, Q
- Output – D

Design of a Clocked JK Latch – Version II



Block Diagram

Clk	J	K	Qn	Qn+1	D
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	0

Truth Table

Clk	J	K	Action	Q_{N+1}
0	x	x	Hold	Q_N
1	0	0	Hold	Q_N
1	0	1	Reset	0
1	1	0	Set	1
1	1	1	Toggle	$\overline{Q}_N$

Function Table

$Q_n \rightarrow Q_{n+1}$	D
$0 \rightarrow 0$	0
$0 \rightarrow 1$	1
$1 \rightarrow 0$	0
$1 \rightarrow 1$	1

Excitation Table

$$D = \overline{K} \cdot Q + Q \cdot \overline{clk} + clk \cdot J \cdot \overline{Q}$$

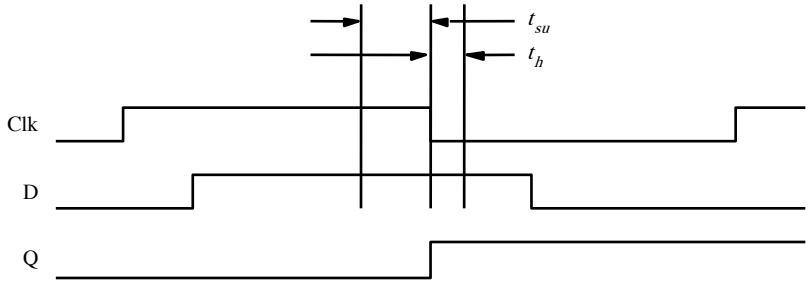
Equation

Terminology

- Latches are often called ***Transparent*** because the output will follow the input as long as the clock signal is high.
- Flip-flops are ***edge-triggered***
  - Positive-edge triggered (PET) is when action occurs on the rising edge of the clock signal;
  - Negative-edge triggered (NET) is when action occurs on the falling edge of the clock signal.
- Types of Flip-flops
  - SR (rarely used);
  - D (very, very common, 74HC74);
  - JK (hardly ever used, 74HC109);
  - Toggle (occasionally used by CAD programs).

Setup and Hold Times

- Setup time (t_{SU}) is the time interval preceding the active transition point of the CLK during which all data inputs must remain stable.
- Hold time (t_H) is the time interval following the active transition point of the CLK during which all data inputs must remain stable.
- See data sheet for 74HC74



PET Master-Slave D Flip-Flop

- QM follows the D input whenever CLK is low.
- When CLK goes high, QM is transferred to the output.

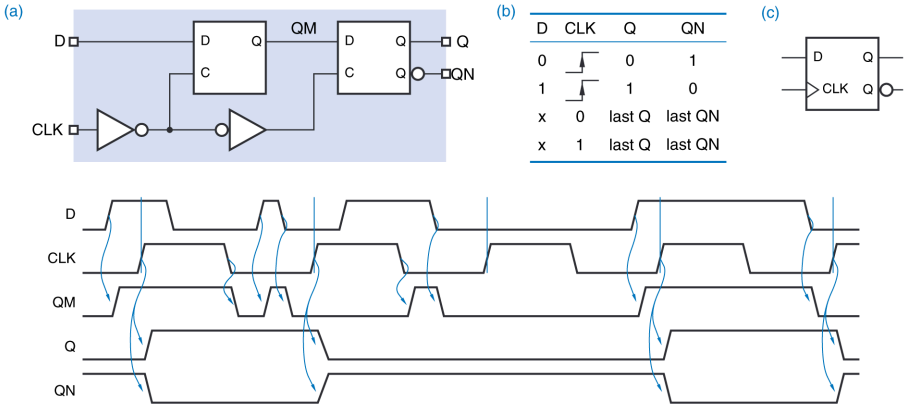


Figure 7-16
Functional behavior of a positive-edge-triggered D flip-flop.

Positive-Edge-Triggered D Flip-Flop

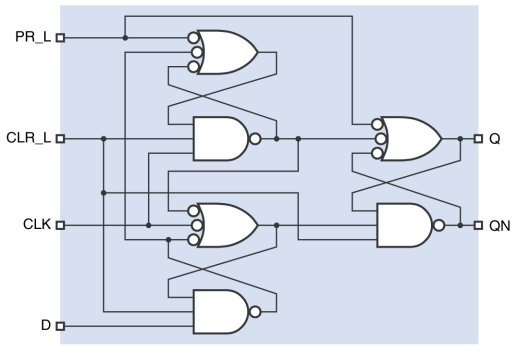


Figure 7-20
Commercial circuit for a positive-edge-triggered D flip-flop such as 74LS74.

PET D Flip-Flop with *Clear* and *Preset*

- Synchronous – transitions or actions occur in relation to the CLK signal;
- Asynchronous – transitions or actions are not related to the CLK signal.

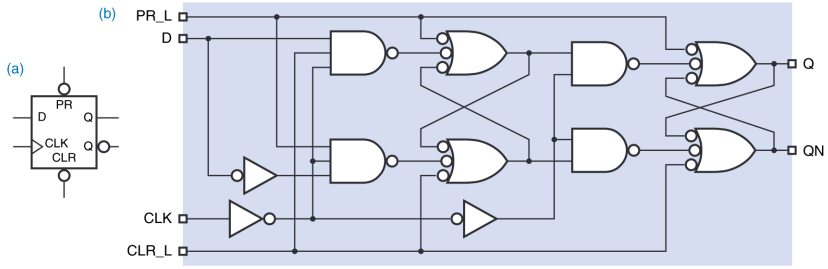
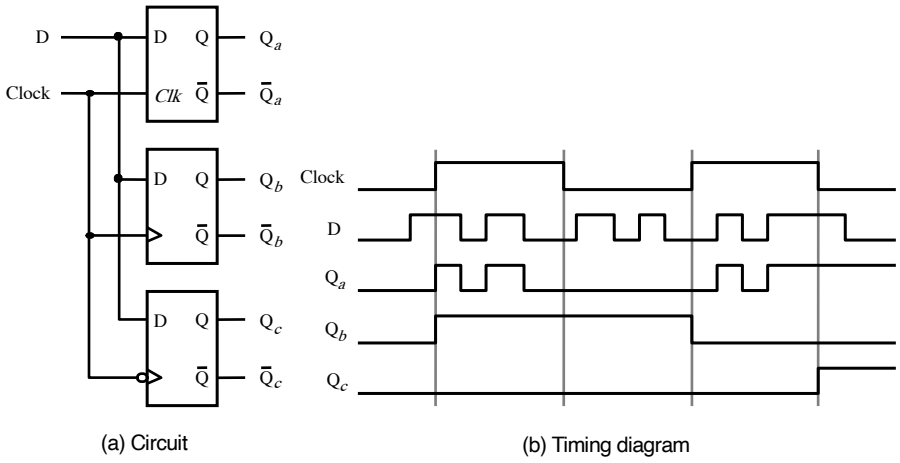


Figure 7-19
Positive-edge-triggered D flip-flop with preset and clear:
(a) logic symbol; (b) circuit design using NAND gates.

Level-Sensitive vs. Edge-Triggered

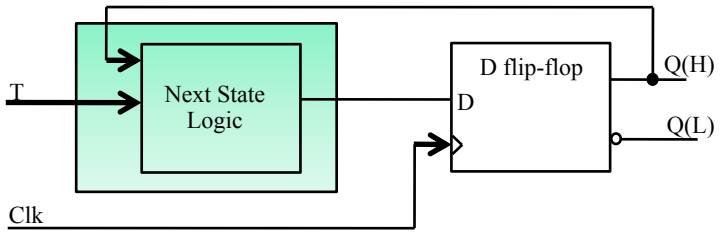
- Level-sensitive = latch
- Edge-triggered = flip-flop



(a) Circuit (b) Timing diagram

Design a T Flip-Flop from a D Flip-Flop

- The memory element is now ***edge-triggered*** meaning the Clk signal is no longer part of the ***next-state logic***.



T	Q(n + 1)
0	$Q(n)$
1	$\bar{Q}(n)$

Function Table

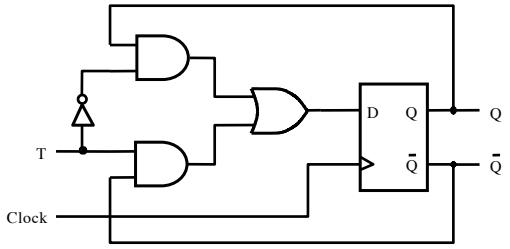
$Q_n \rightarrow Q_{n+1}$	D
$0 \rightarrow 0$	0
$0 \rightarrow 1$	1
$1 \rightarrow 0$	0
$1 \rightarrow 1$	1

Excitation Table

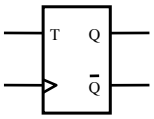
T	Qn	Qn+1	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Truth Table

Design a T Flip-Flop from a D Flip-Flop

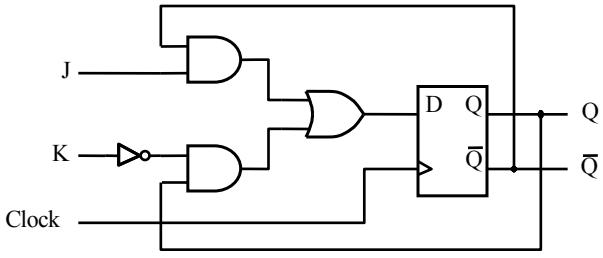


(a) Circuit



(c) Graphical symbol

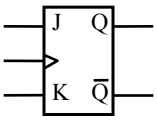
Design a JK Flip-Flop from a D Flip-Flop



Circuit

J	K	Q(n+1)
0	0	Q(n)
0	1	0
1	0	1
1	1	$\overline{Q}$(n)

Function Table



Graphical symbol

Summary of Terminology

- Basic cell – cross-coupled NAND/NOR.
- Gated latch – output changes only when *Clk* is asserted
  - Gated SR latch;
  - Gated D latch;
  - Gated JK latch.
- Flip-flop – output changes only on *Clk* edge
  - Master-slave;
  - Edge-triggered;
  - Three main types
    - D (very, very common, 74HC74);
    - JK (hardly ever used, 74HC109);
    - Toggle (occasionally used by CAD programs).

Sequential Logic Elements Summary

In this chapter you learned about

- Logic circuits that can store information;
- Basic cells, latches, and flip-flops;
- State diagrams;
- Design techniques for circuits that use flip-flops.