Engr354 **Exam #2**

NAME KEY SCORE _____/50

This is a closed book test. One sheet of private reference is allowed.

Circle T or F below. One point per problem.

(T) F In *combinational* circuits, the outputs depends only on the inputs.

(T) F In a synchronous state machine, the *Present State* is found at the outputs of the flip-flops.

T (F) A synchronous reset will reset the output of a flip-flop independent of the state of the clock signal.

(T) F The clock input to a synchronous state machine is an asynchronous signal.

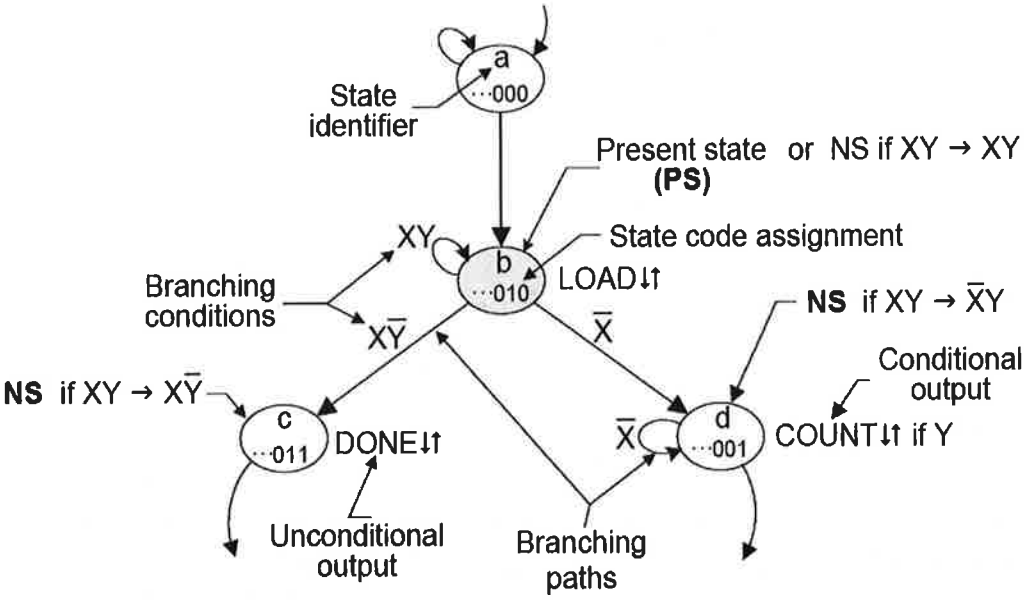
Answer the following problems for the state diagram shown below. One point per problem.

List the input(s). X and Y

List the output(s). LOAD, DONE, COUNT

List the next states of the 010 state. 010, 001, 011
or b d c

List the previous states of the [redacted] state. a b
010 000 010

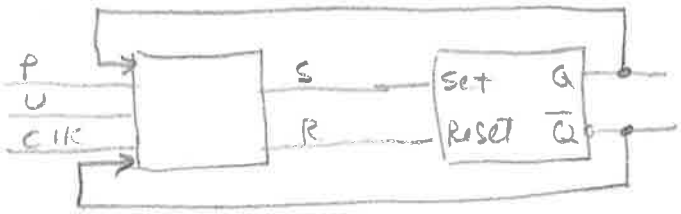


15 pts Latch Design

Design a latch that uses the combined version of the basic cell, as developed in class, as a storage element (excitation table shown below). This latch has two inputs, **P** and **U**, in addition to a **clk** signal which acts as a gate. The output should hold if either P or U is a 0 (00, 01, 10) and toggle if P and U are both 1 (function table shown below). Create the following items in your design:

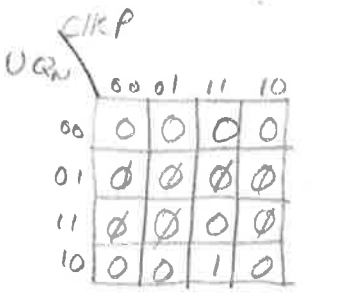
a. Block diagram showing inputs and outputs
b. Truth table for the next state logic
c. Minimized equations for the inputs to the basic cell
d. You do not need to draw a schematic

P U	Action
0 0	Hold
0 1	Hold
1 0	Hold
1 1	Toggle

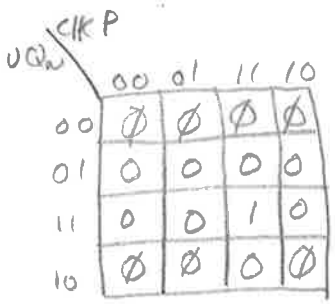


$Q_n \rightarrow Q_{n+1}$	S R
0 0	0 Ø
0 1	1 0
1 0	0 1
1 1	Ø 0

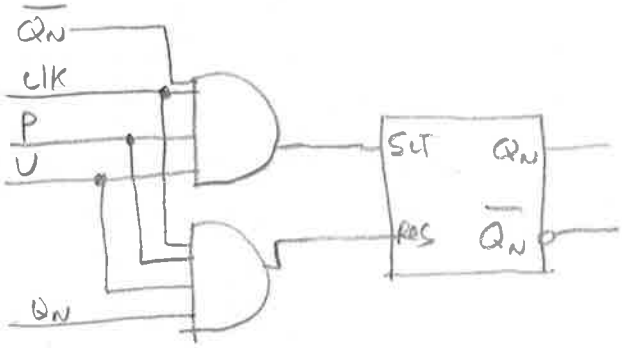
CLK	P	U	Q_N	Q_{N+1}	S	R
0	0	0	0	0	0	Ø
0	0	0	1	1	Ø	0
0	0	1	0	0	0	Ø
0	0	1	1	1	Ø	0
0	1	0	0	0	0	Ø
0	1	0	1	1	Ø	0
0	1	1	0	0	0	Ø
0	1	1	1	1	Ø	0
1	0	0	0	0	0	Ø
1	0	0	1	1	Ø	0
1	0	1	0	0	0	Ø
1	0	1	1	1	Ø	0
1	1	0	0	0	0	Ø
1	1	0	1	1	Ø	0
1	1	1	0	1	0	1
1	1	1	1	0	1	0



$S = CLK \cdot P \cdot U \cdot \overline{Q_N}$

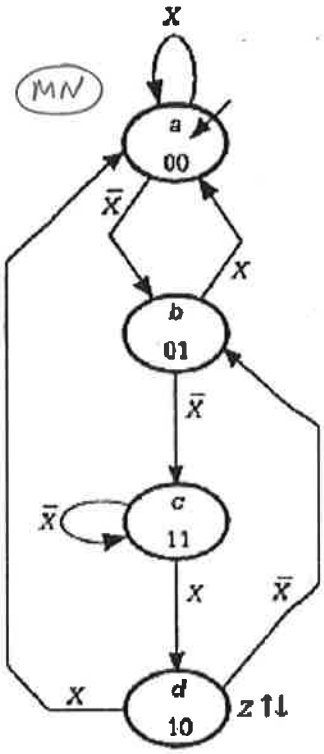


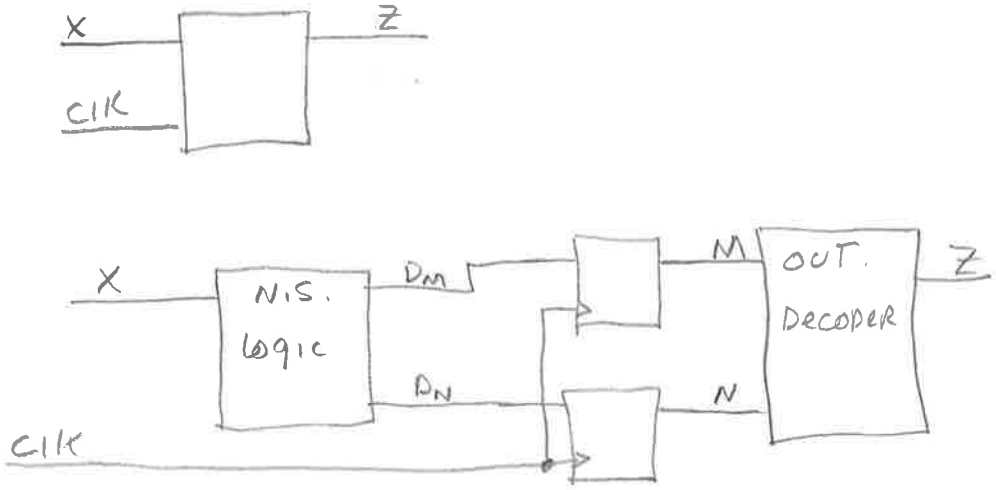
$R = CLK \cdot P \cdot U \cdot Q_N$

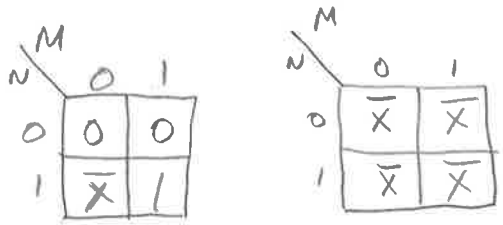


15 pts State Machine Design

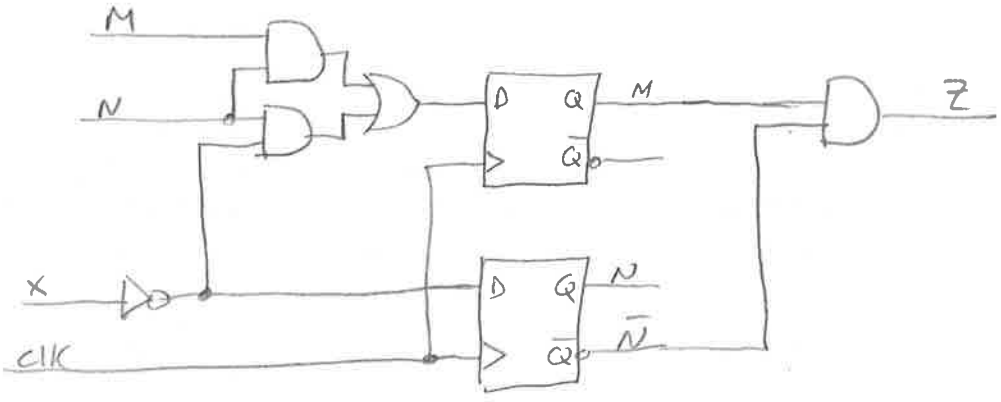
Using rising edge-triggered D flip-flops, design and construct a **minimum** logic state-machine that implements the state diagram shown at the right. Create next state maps and minimum expressions for the next state variables and output(s). Draw the circuit you designed, make it readable, not necessarily pretty. Assume all inputs and outputs are active high.



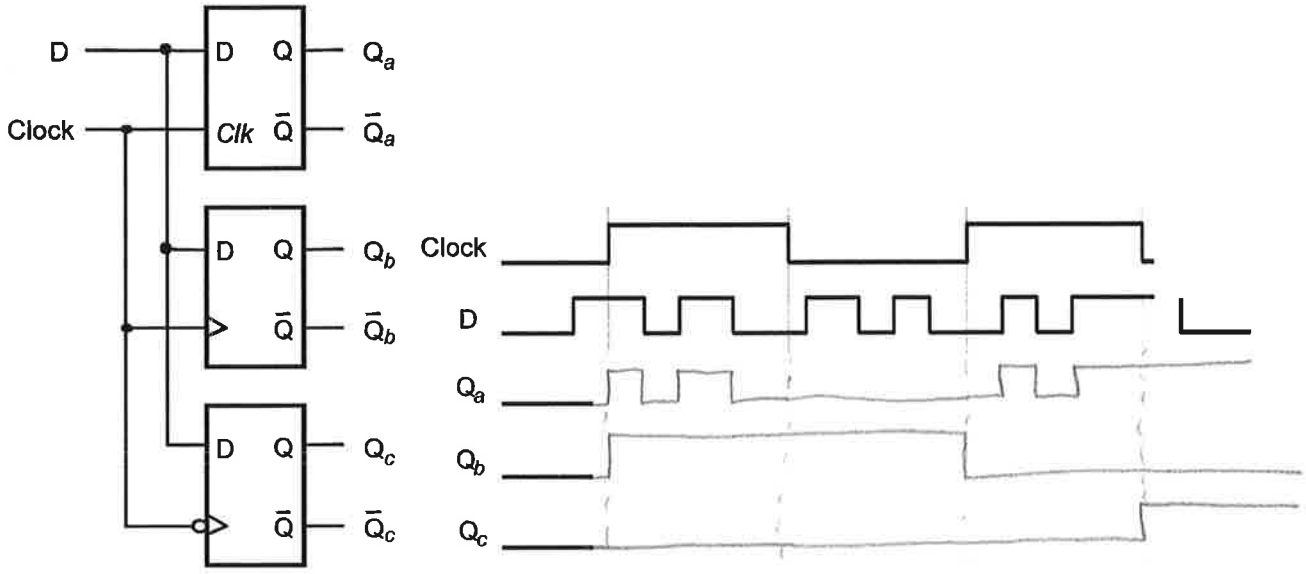




$M = MN + N\bar{X}$ $N = \bar{X}$ $Z = M\bar{N}$



8 pts Given the circuit below, fill in the timing diagram for the three outputs, Q_a, Q_b, and Q_c.



(a) Circuit

(b) Timing diagram