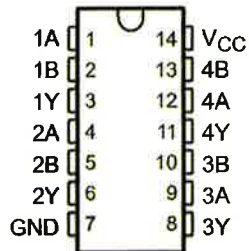


SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

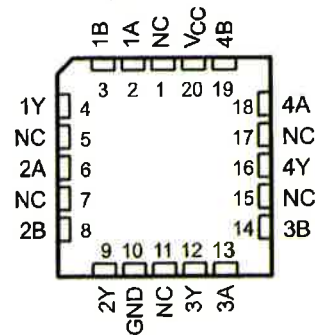
SCLS181E – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 8$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC00 . . . J OR W PACKAGE
SN74HC00 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC00 devices contain four independent 2-input NAND gates. They perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC00N	SN74HC00N
		Tube of 50	SN74HC00D	HC00
	SOIC – D	Reel of 2500	SN74HC00DR	
		Reel of 250	SN74HC00DT	
	SOP – NS	Reel of 2000	SN74HC00NSR	HC00
	SSOP – DB	Reel of 2000	SN74HC00DBR	HC00
	TSSOP – PW		Tube of 90	SN74HC00PW
Reel of 2000			SN74HC00PWR	
Reel of 250			SN74HC00PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC00J	SNJ54HC00J
	CFP – W	Tube of 150	SNJ54HC00W	SNJ54HC00W
	LCCC – FK	Tube of 55	SNJ54HC00FK	SNJ54HC00FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SCLS181E – DECEMBER 1982 – REVISED AUGUST 2003

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HC00			SN74HC00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5	1.5		V	
		$V_{CC} = 4.5\text{ V}$		3.15	3.15			
		$V_{CC} = 6\text{ V}$		4.2	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$			0.5		V	
		$V_{CC} = 4.5\text{ V}$			1.35			
		$V_{CC} = 6\text{ V}$			1.8			
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2\text{ V}$			1000		ns	
		$V_{CC} = 4.5\text{ V}$			500			
		$V_{CC} = 6\text{ V}$			400			
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

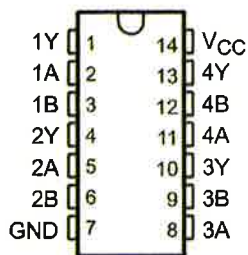


SN54HC02, SN74HC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

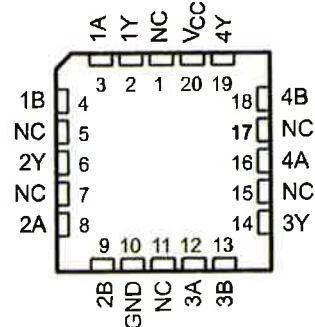
SCLS076E – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 8$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC02 . . . J OR W PACKAGE
SN74HC02 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC02 devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC02N	SN74HC02N
	SOIC – D	Tube of 50	SN74HC02D	HC02
		Reel of 2500	SN74HC02DR	
		Reel of 250	SN74HC02DT	
	SOP – NS	Reel of 2000	SN74HC02NSR	HC02
	SSOP – DB	Reel of 2000	SN74HC02DBR	HC02
	TSSOP – PW	Tube of 90	SN74HC02PW	HC02
Reel of 2000		SN74HC02PWR		
Reel of 250		SN74HC02PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC02J	SNJ54HC02J
	CFP – W	Tube of 150	SNJ54HC02W	SNJ54HC02W
	LCCC – FK	Tube of 55	SNJ54HC02FK	SNJ54HC02FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC02, SN74HC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS076E – DECEMBER 1982 – REVISED AUGUST 2003

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HC02			SN74HC02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5		V	
		$V_{CC} = 4.5$ V			1.35			
		$V_{CC} = 6$ V			1.8			
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V			1000		ns	
		$V_{CC} = 4.5$ V			500			
		$V_{CC} = 6$ V			400			
T_A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



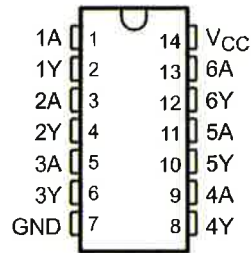
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SN54HC04, SN74HC04 HEX INVERTERS

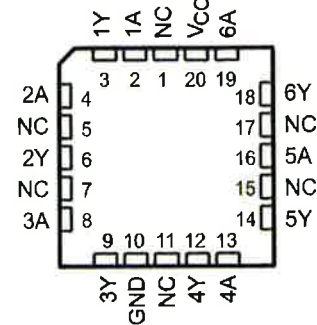
SCLS078D – DECEMBER 1982 – REVISED JULY 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 8$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC04 . . . J OR W PACKAGE
SN74HC04 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC04 devices contain six independent inverters. They perform the Boolean function $Y = \bar{A}$ in positive logic.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC04N	SN74HC04N
		Tube of 50	SN74HC04D	HC04
	SOIC – D	Reel of 2500	SN74HC04DR	
		Reel of 250	SN74HC04DT	
	SOP – NS	Reel of 2000	SN74HC04NSR	
	TSSOP – PW		Tube of 90	SN74HC04PW
Reel of 2000			SN74HC04PWR	
Reel of 250			SN74HC04PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC04J	SNJ54HC04J
	CFP – W	Tube of 150	SNJ54HC04W	SNJ54HC04W
	LCCC – FK	Tube of 55	SNJ54HC04FK	SNJ54HC04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H



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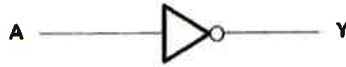
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SN54HC04, SN74HC04 HEX INVERTERS

SCLS078D – DECEMBER 1982 – REVISED JULY 2003

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HC04			SN74HC04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5		V	
		$V_{CC} = 4.5$ V			1.35			
		$V_{CC} = 6$ V			1.8			
V_I	Input voltage	0		V_{CC}	0	V_{CC}	V	
V_O	Output voltage	0		V_{CC}	0	V_{CC}	V	
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V			1000		ns	
		$V_{CC} = 4.5$ V			500			
		$V_{CC} = 6$ V			400			
T_A	Operating free-air temperature	-55		125	-40	85	°C	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

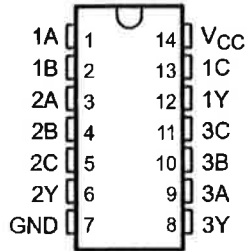


SN54HC10, SN74HC10 TRIPLE 3-INPUT POSITIVE-NAND GATES

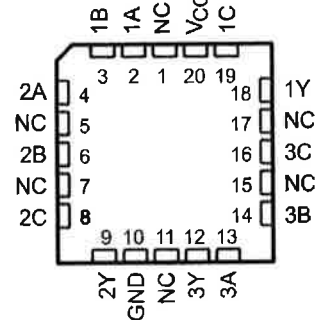
SCLS083D - DECEMBER 1982 - REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 9$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC10 . . . J OR W PACKAGE
SN74HC10 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC10 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description/ordering information

The 'HC10 devices contain three independent 3-input NAND gates. They perform the Boolean function $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP - N	Tube of 25	SN74HC10N	SN74HC10N
	SOIC - D	Tube of 50	SN74HC10D	HC10
		Reel of 2500	SN74HC10DR	
		Reel of 250	SN74HC10DT	
	SOP - NS	Reel of 2000	SN74HC10NSR	HC10
	SSOP - DB	Reel of 2000	SN74HC10DBR	HC10
	TSSOP - PW	Tube of 90	SN74HC10PW	HC10
Reel of 2000		SN74HC10PWR		
Reel of 250		SN74HC10PWT		
-55°C to 125°C	CDIP - J	Tube of 25	SNJ54HC10J	SNJ54HC10J
	CFP - W	Tube of 150	SNJ54HC10W	SNJ54HC10W
	LCCC - FK	Tube of 55	SNJ54HC10FK	SNJ54HC10FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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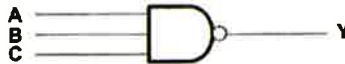
SN54HC10, SN74HC10 TRIPLE 3-INPUT POSITIVE-NAND GATES

SCLS083D - DECEMBER 1982 - REVISED AUGUST 2003

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

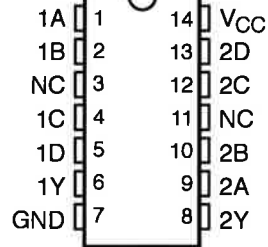
- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC20, SN74HC20 DUAL 4-INPUT POSITIVE-NAND GATES

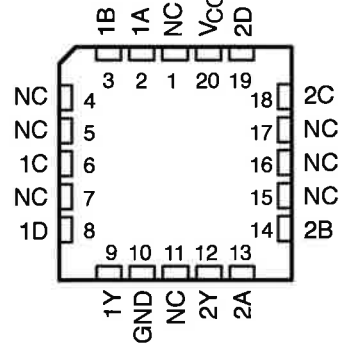
SCLS086F – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 11$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC20 . . . J OR W PACKAGE
SN74HC20 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC20 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC20 devices contain two independent 4-input NAND gates. They perform the Boolean function $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A + B + C + D}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC20N	SN74HC20N
		Tube of 50	SN74HC20D	HC20
	SOIC – D	Reel of 2500	SN74HC20DR	
		Reel of 250	SN74HC20DT	
	SOP – NS	Reel of 2000	SN74HC20NSR	HC20
	SSOP – DB	Reel of 2000	SN74HC20DBR	HC20
	TSSOP – PW	Tube of 90	SN74HC20PW	HC20
Reel of 2000		SN74HC20PWR		
Reel of 250		SN74HC20PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC20J	SNJ54HC20J
	CFP – W	Tube of 150	SNJ54HC20W	SNJ54HC20W
	LCCC – FK	Tube of 55	SNJ54HC20FK	SNJ54HC20FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC20, SN74HC20 DUAL 4-INPUT POSITIVE-NAND GATES

SCLS086F – DECEMBER 1982 – REVISED AUGUST 2003

FUNCTION TABLE
(each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

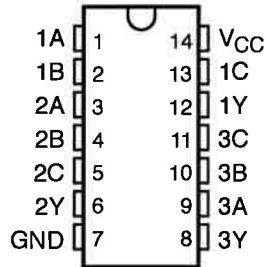
Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

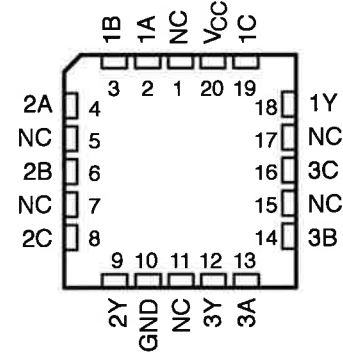
- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 9$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC27 . . . J OR W PACKAGE
SN74HC27 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



SN54HC27 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC27 devices contain three independent 3-input NOR gates. They perform the Boolean function $Y = A + B + C$ or $Y = \bar{A} \cdot \bar{B} \cdot \bar{C}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC27N	SN74HC27N
		Tube of 50	SN74HC27D	HC27
	SOIC – D	Reel of 2500	SN74HC27DR	
		Reel of 250	SN74HC27DT	
	SOP – NS	Reel of 2000	SN74HC27NSR	HC27
SSOP – DB	Reel of 2000	SN74HC27DBR	HC27	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC27J	SNJ54HC27J
	CFP – W	Tube of 150	SNJ54HC27W	SNJ54HC27W
	LCCC – FK	Tube of 55	SNJ54HC27FK	SNJ54HC27FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H



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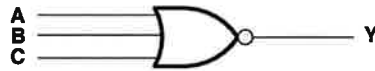
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SN54HC27, SN74HC27 TRIPLE 3-INPUT POSITIVE-NOR GATES

SCLS088D – DECEMBER 1982 – REVISED AUGUST 2003

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal Impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HC27			SN74HC27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	$V_{CC} = 6$ V		4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5	$V_{CC} = 2$ V		0.5
		$V_{CC} = 4.5$ V			1.35	$V_{CC} = 4.5$ V		1.35
		$V_{CC} = 6$ V			1.8	$V_{CC} = 6$ V		1.8
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V			1000	$V_{CC} = 2$ V		1000
		$V_{CC} = 4.5$ V			500	$V_{CC} = 4.5$ V		500
		$V_{CC} = 6$ V			400	$V_{CC} = 6$ V		400
T_A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54HC74, SN74HC74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

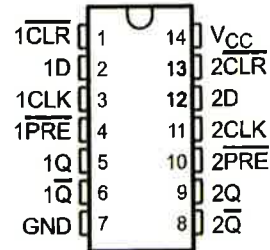
SCLS094D – DECEMBER 1982 – REVISED JULY 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 40- μ A Max I_{CC}
- Typical $t_{pd} = 15$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

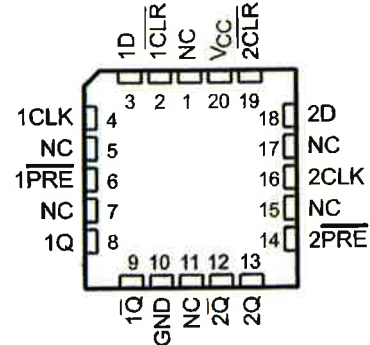
description/ordering information

The 'HC74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

SN54HC74 ... J OR W PACKAGE
SN74HC74 ... D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC74 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC74N	
	SOIC – D	Tube of 50	SN74HC74D	HC74
		Reel of 2500	SN74HC74DR	
		Reel of 250	SN74HC74DT	
		SOP – NS	Reel of 2000	
	SSOP – DB	Reel of 2000	SN74HC74DBR	HC74
	TSSOP – PW	Tube of 90	SN74HC74PW	HC74
Reel of 2000		SN74HC74PWR		
Reel of 250		SN74HC74PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC74J	
	CFP – W	Tube of 150	SNJ54HC74W	
	LCCC – FK	Tube of 55	SNJ54HC74FK	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC74, SN74HC74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

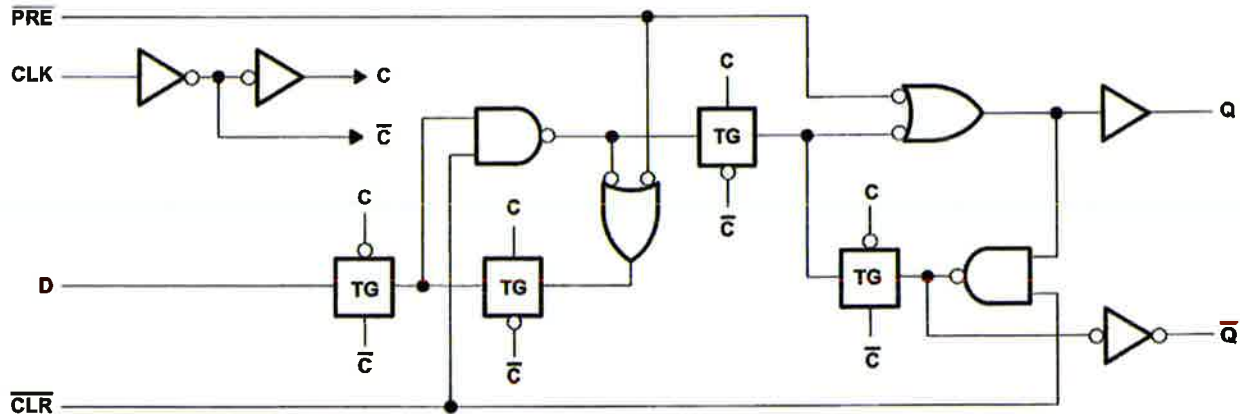
SCLS094D – DECEMBER 1982 – REVISED JULY 2003

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q} ₀

[†] This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



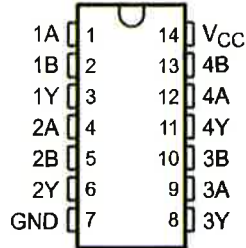
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SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

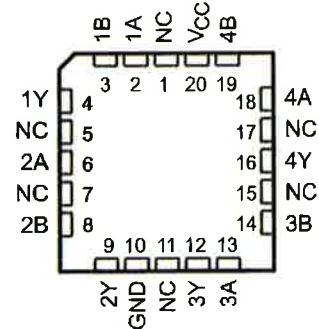
SCLS100E – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 10$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- True Logic

SN54HC86 . . . J OR W PACKAGE
SN74HC86 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC86N	SN74HC86N
		Tube of 50	SN74HC86D	HC86
	SOIC – D	Reel of 2500	SN74HC86DR	
		Reel of 250	SN74HC86DT	
	SOP – NS	Reel of 2000	SN74HC86NSR	
	TSSOP – PW		Tube of 90	SN74HC86PW
Reel of 2000			SN74HC86PWR	
Reel of 250			SN74HC86PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC86J	SNJ54HC86J
	CFP – W	Tube of 150	SNJ54HC86W	SNJ54HC86W
	LCCC – FK	Tube of 55	SNJ54HC86FK	SNJ54HC86FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS100E – DECEMBER 1982 – REVISED AUGUST 2003

FUNCTION TABLE
(each gate)

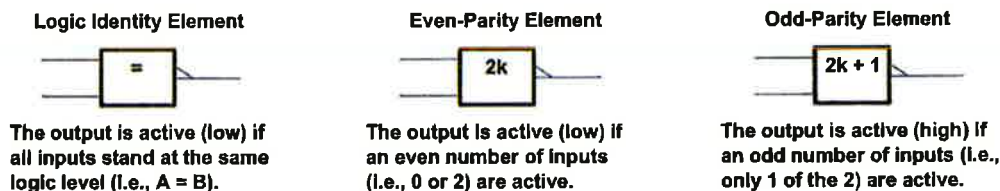
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

October 1997 - Revised August 2004

**High-Speed CMOS Logic 3- to 8-Line Decoder/
Demultiplexer Inverting and Noninverting**
Features

- **Select One Of Eight Data Outputs**
Active Low for 138, Active High for 238
- **I/O Port or Memory Selector**
- **Three Enable Inputs to Simplify Cascading**
- **Typical Propagation Delay of 13 ns at $V_{CC} = 5\text{ V}$,
 $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$**
- **Fanout (Over Temperature Range)**
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL
Logic ICs**
- **HC Types**
 - 2 V to 6 V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}
at $V_{CC} = 5\text{ V}$
- **HCT Types**
 - 4.5-V to 5.5-V Operation
 - Direct LSTTL Input Logic Compatibility,
 $V_{IL} = 0.8\text{ V (Max)}$, $V_{IH} = 2\text{ V (Min)}$
 - CMOS Input Compatibility, $I_i \leq 1\mu\text{A}$ at V_{OL} , V_{OH}

Description

The 'HC138, 'HC238, 'HCT138, and 'HCT238 are high-speed silicon-gate CMOS decoders well suited to memory address decoding or data-routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low-power Schottky TTL logic. Both circuits have three binary select inputs (A0, A1, and A2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC/HCT138 series go low or which of the normally low outputs of the HC/HCT238 series go high.

Two active low and one active high enables ($\overline{E1}$, $\overline{E2}$, and E3) are provided to ease the cascading of decoders. The decoder's eight outputs can drive ten low-power Schottky TTL equivalent loads.

Ordering Information

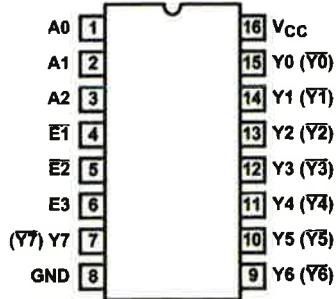
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC138F3A	-55 to 125	16 Ld CERDIP
CD54HC238F3A	-55 to 125	16 Ld CERDIP
CD54HCT138F3A	-55 to 125	16 Ld CERDIP
CD54HCT238F3A	-55 to 125	16 Ld CERDIP
CD74HC138E	-55 to 125	16 Ld PDIP
CD74HC138M	-55 to 125	16 Ld SOIC
CD74HC138MT	-55 to 125	16 Ld SOIC
CD74HC138M96	-55 to 125	16 Ld SOIC
CD74HC238E	-55 to 125	16 Ld PDIP
CD74HC238M	-55 to 125	16 Ld SOIC
CD74HC238MT	-55 to 125	16 Ld SOIC
CD74HC238M96	-55 to 125	16 Ld SOIC
CD74HC238NSR	-55 to 125	16 Ld SOP
CD74HC238PW	-55 to 125	16 Ld TSSOP
CD74HC238PWR	-55 to 125	16 Ld TSSOP
CD74HC238PWT	-55 to 125	16 Ld TSSOP
CD74HCT138E	-55 to 125	16 Ld PDIP
CD74HCT138M	-55 to 125	16 Ld SOIC
CD74HCT138MT	-55 to 125	16 Ld SOIC
CD74HCT138M96	-55 to 125	16 Ld SOIC
CD74HCT238E	-55 to 125	16 Ld PDIP
CD74HCT238M	-55 to 125	16 Ld SOIC
CD74HCT238M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

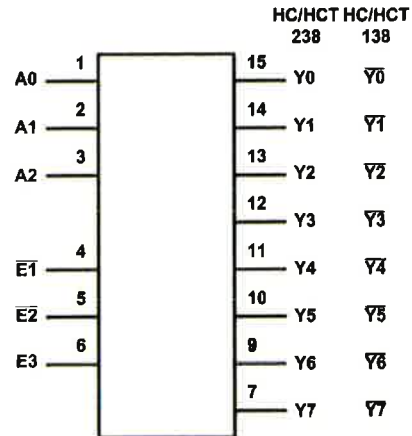
CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

Pinout

CD54HC138, CD54HCT138, CD54HC238, CD54HCT238
(CERDIP)
CD74HC138, CD74HCT138, CD74HCT238
(PDIP, SOIC)
CD74HC238
(PDIP, SOIC, SOP, TSSOP)
TOP VIEW



Functional Diagram



Signal names in parentheses are for 'HC138 and 'HCT138.

TRUTH TABLE 'HC138, 'HCT138

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

TRUTH TABLE 'HC238, 'HCT238

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

SN54HC139, SN74HC139

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

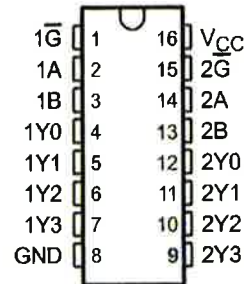
SCLS108D - DECEMBER 1982 - REVISED SEPTEMBER 2003

- Targeted Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 10$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception

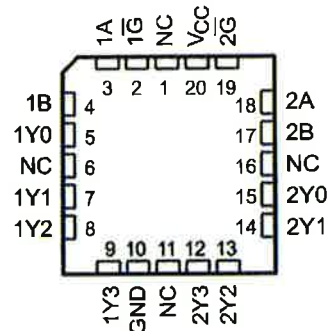
description/ordering information

The 'HC139 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

SN54HC139 . . . J OR W PACKAGE
SN74HC139 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC139 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

T_A	PACKAGE†	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP - N	Tube of 25	SN74HC139N	SN74HC139N
	SOIC - D	Tube of 40	SN74HC139D	HC139
		Reel of 2500	SN74HC139DR	
		Reel of 250	SN74HC139DT	
		SOP - NS	Reel of 2000	
	SSOP - DB	Reel of 2000	SN74HC139DBR	HC139
-55°C to 125°C	TSSOP - PW	Tube of 90	SN74HC139PW	HC139
		Reel of 2000	SN74HC139PWR	
		Reel of 250	SN74HC139PWT	
-55°C to 125°C	CDIP - J	Tube of 25	SNJ54HC139J	SNJ54HC139J
	CFP - W	Tube of 150	SNJ54HC139W	SNJ54HC139W
	LCCC - FK	Tube of 55	SNJ54HC139FK	SNJ54HC139FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC139, SN74HC139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCLS108D - DECEMBER 1982 - REVISED SEPTEMBER 2003

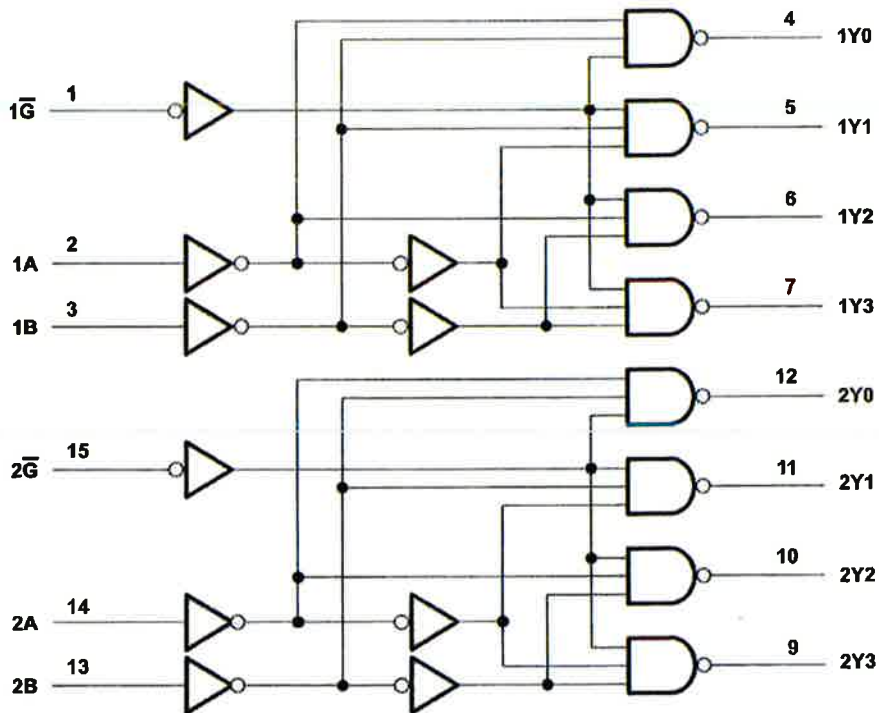
description/ordering information (continued)

The 'HC139 devices comprise two individual 2-line to 4-line decoders in a single package. The active-low enable (\bar{G}) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

FUNCTION TABLE

\bar{G}	INPUTS		OUTPUTS			
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.



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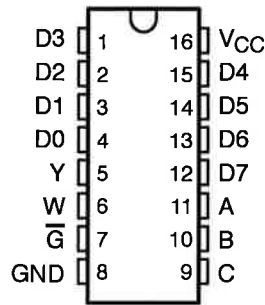
SN54HC151, SN74HC151

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

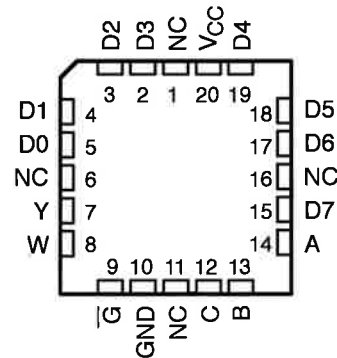
SCLS110E – DECEMBER 1982 – REVISED SEPTEMBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- 8-Line to 1-Line Multiplexers Can Perform as:
 - Boolean-Function Generators
 - Parallel-to-Serial Converters
 - Data Source Selectors

SN54HC151 . . . J OR W PACKAGE
SN74HC151 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC151 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe (\bar{G}) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC151N	SN74HC151N
	SOIC – D	Tube of 40	SN74HC151D	HC151
		Reel of 2500	SN74HC151DR	
		Reel of 250	SN74HC151DT	
	SOP – NS	Reel of 2000	SN74HC151NSR	HC151
	TSSOP – PW	Tube of 90	SN74HC151PW	HC151
Reel of 2000		SN74HC151PWR		
Reel of 250		SN74HC151PWT		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC151J	SNJ54HC151J
	CFP – W	Tube of 150	SNJ54HC151W	SNJ54HC151W
	LCCC – FK	Tube of 55	SNJ54HC151FK	SNJ54HC151FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC151, SN74HC151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS110E - DECEMBER 1982 - REVISED SEPTEMBER 2003

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE G	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

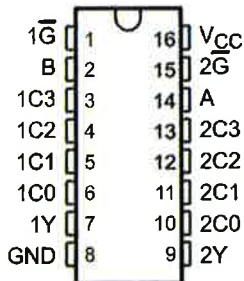
D0, D1 . . . D7 = the level of the respective D input

SN54HC153, SN74HC153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

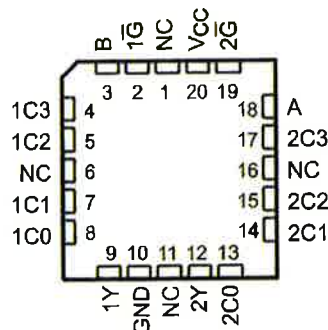
SCLS112D - DECEMBER 1982 - REVISED OCTOBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 9$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Permit Multiplexing from n Lines to One Line
- Perform Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)

SN54HC153 ... J OR W PACKAGE
SN74HC153 ... D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC153 ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

description/ordering information

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe (\bar{G}) inputs are provided for each of the two 4-line sections.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP - N	Tube of 25	SN74HC153N	SN74HC153N
	SOIC - D	Tube of 40	SN74HC153D	HC153
		Reel of 2500	SN74HC153DR	
		Reel of 250	SN74HC153DT	
	SOP - NS	Reel of 2000	SN74HC153NSR	HC153
	TSSOP - PW	Tube of 90	SN74HC153PW	HC153
Reel of 2000		SN74HC153PWR		
Reel of 250		SN74HC153PWT		
-55°C to 125°C	CDIP - J	Tube of 25	SNJ54HC153J	SNJ54HC153J
	CFP - W	Tube of 150	SNJ54HC153W	SNJ54HC153W
	LCCC - FK	Tube of 55	SNJ54HC153FK	SNJ54HC153FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC153, SN74HC153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS112D - DECEMBER 1982 - REVISED OCTOBER 2003

FUNCTION TABLE

INPUTS							OUTPUT Y
SELECT†		DATA				\bar{G}	
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

† Select inputs A and B are common to both sections.



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The CD54HCT161 is obsolete and no longer is supplied.

CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

Data sheet acquired from Harris Semiconductor
SCHS154D

High-Speed CMOS Logic Presettable Counters

February 1998 - Revised October 2003

Features

- 'HC161, 'HCT161 4-Bit Binary Counter, Asynchronous Reset
- 'HC163, 'HCT163 4-Bit Binary Counter, Synchronous Reset
- Synchronous Counting and Loading
- Two Count Enable Inputs for n-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC161, 'HCT161, 'HC163, and 'HCT163 are presettable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The 'HC161 and 'HCT161 are asynchronous reset decade and binary counters, respectively; the 'HC163 and 'HCT163 devices are decade and binary counters, respectively, that are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A low level on the synchronous parallel enable input, SPE, disables counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for SPE are met).

All counters are reset with a low level on the Master Reset input, MR. In the 'HC163 and 'HCT163 counters (synchronous reset types), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. In all counters reset action occurs regardless of the level of the \overline{SPE} , PE and TE inputs (and the clock input, CP, in the 'HC161 and 'HCT161 types).

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be high to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count the terminal count (TC) output goes high for one clock period. This TC pulse is used to enable the next cascaded stage.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC161F3A	-55 to 125	16 Ld CERDIP
CD54HC163F3A	-55 to 125	16 Ld CERDIP
CD54HCT163F3A	-55 to 125	16 Ld CERDIP
CD74HC161E	-55 to 125	16 Ld PDIP
CD74HC161M	-55 to 125	16 Ld SOIC
CD74HC161MT	-55 to 125	16 Ld SOIC
CD74HC161M96	-55 to 125	16 Ld SOIC
CD74HC163E	-55 to 125	16 Ld PDIP
CD74HC163M	-55 to 125	16 Ld SOIC
CD74HC163MT	-55 to 125	16 Ld SOIC
CD74HC163M96	-55 to 125	16 Ld SOIC
CD74HCT161E	-55 to 125	16 Ld PDIP
CD74HCT161M	-55 to 125	16 Ld SOIC
CD74HCT161MT	-55 to 125	16 Ld SOIC
CD74HCT161M96	-55 to 125	16 Ld SOIC
CD74HCT163E	-55 to 125	16 Ld PDIP
CD74HCT163M	-55 to 125	16 Ld SOIC
CD74HCT163MT	-55 to 125	16 Ld SOIC
CD74HCT163M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

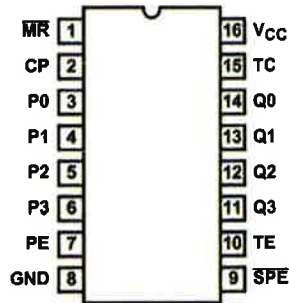
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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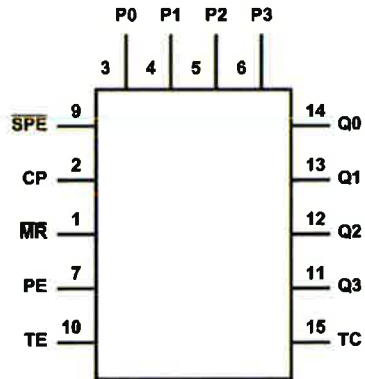
CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

Pinout

CD54HC161, CD54HCT161, CD54HC163, CD54HCT163
(CERDIP)
CD74HC161, CD74HCT161, CD74HC163, CD74HCT163
(PDIP, SOIC)
TOP VIEW



Functional Diagram



CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

MODE SELECT - FUNCTION TABLE FOR 'HC161 AND 'HCT161

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	PE	TE	\overline{SPE}	P_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(Note 1)
Count	H	↑	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	q_n	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	q_n	L

MODE SELECT - FUNCTION TABLE FOR 'HC163 AND 'HCT163

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	PE	TE	\overline{SPE}	P_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h (Note 3)	↑	X	X	l	l	L	L
	h (Note 3)	↑	X	X	l	h	H	(Note 1)
Count	h (Note 3)	↑	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	h (Note 3)	X	l (Note 2)	X	h (Note 3)	X	q_n	(Note 1)
	h (Note 3)	X	X	l (Note 2)	h (Note 3)	X	q_n	L

H = High voltage level steady state; L = Low voltage level steady state; h = High voltage level one setup time prior to the Low-to-High clock transition; l = Low voltage level one setup time prior to the Low-to-High clock transition; X = Don't Care; q_n = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition; ↑ = Low-to-High clock transition.

NOTES:

1. The TC output is High when TE is High and the counter is at Terminal Count (HHHH for HC/HCT161 and 'HC/HCT163).
2. The High-to-Low transition of PE or TE on the 'HC/HCT161 and the 'HC/HCT163 should only occur while CP is HIGH for conventional operation.
3. The Low-to-High transition of \overline{SPE} on the 'HC/HCT161 and \overline{SPE} or \overline{MR} on the 'HC/HCT163 should only occur while CP is HIGH for conventional operation.

