Engr433 Homework #8

Basic VHDL Language Constructs

Due: Wednesday, October 30, Start of Class

To Do

- Read chapter 3 of the Chu text.
- Do problems 3.1, 3.2, 3.5, and 3.7
- Note: As you learn VHDL you will find capabilities of the language that are useful for synthesizing circuits and other capabilities that are not. The textbook author comments on these at times. Pay close attention to his comments.
- Notes
  - Sections 3.1 to 3.3 give additional details on basics.
  - Read section 3.4 carefully paying particular attention to the description of **Signals**.
  - Section 3.5 is packed with information. Initially, focus on sections 3.5.1 and 3.5.2. Pay particular attention to table 3.1 since it shows available arithmetic and logic operators. The concatenation operator is covered on page 59, middle of the page, and will help with problem 3.7. Scan over the remaining parts of section 3.5 so you know what is there and can refer back to it as you do designs. Note the bottom of page 62 and on thru page 63 where table 3.8 and the examples show various numeric data type conversions.
  - Section 3.6 summarizes guidelines for writing good VHDL descriptions that will synthesize. Scan over this information now but once you have written your own VHDL descriptions, come back to this section and read it again.

To Turn In

Staple this assignment sheet to the front of your solutions, which are to be done in accordance with the school of engineering homework guidelines posted on the course web page. Include:

- Staple!
- Problem statements!