Engr433 Lab #3

Circuit Design with FPGA Implementation

Name _____

Partner _____ **Grade** _____/10

Objectives

- Gain further experience designing state machines;
- Learn how to implement a circuit in a Xilinx FPGA using schematic driven entry tools;
- Refine your
  - Design strategies;
  - Testing approach;
  - Debugging skills.

References

- This handout:
- Xilinx documents on the class web page
  - *Schematic entry using Xilinx tools tutorial*
  - *Xilinx schematic library reference manual for ISE 14.7*

Lab Components Required

- Linux computer with Xilinx software;
- FPGA boards with download and power cables;
- Instruments as necessary.

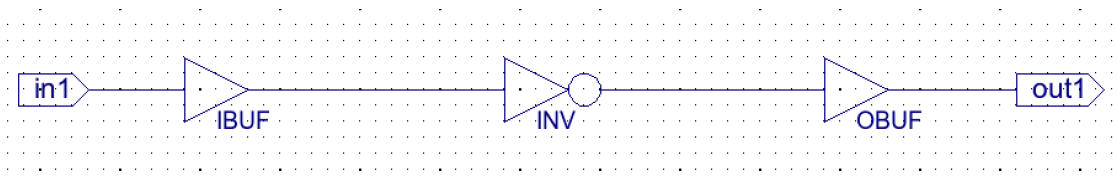
Design Flow

Complete the 3 tasks below using this design flow:

- Enter your schematic design using the Xilinx schematic editor by identifying the necessary library parts;
- Synthesize an FPGA implementation (place, route, and create a bit map file);
- Download the bit map file to the FPGA board;
- Test, debug, and reiterate as needed.

Task 1

Follow the handout entitled *Schematic entry using Xilinx tools tutorial* on the course web page that details schematic driven design with the Xilinx ISE program and create a simple circuit using switch 0 as the input and LED 0 as the output. The purpose of this exercise is to learn to use the Xilinx tools. The schematic you create will look something like this:



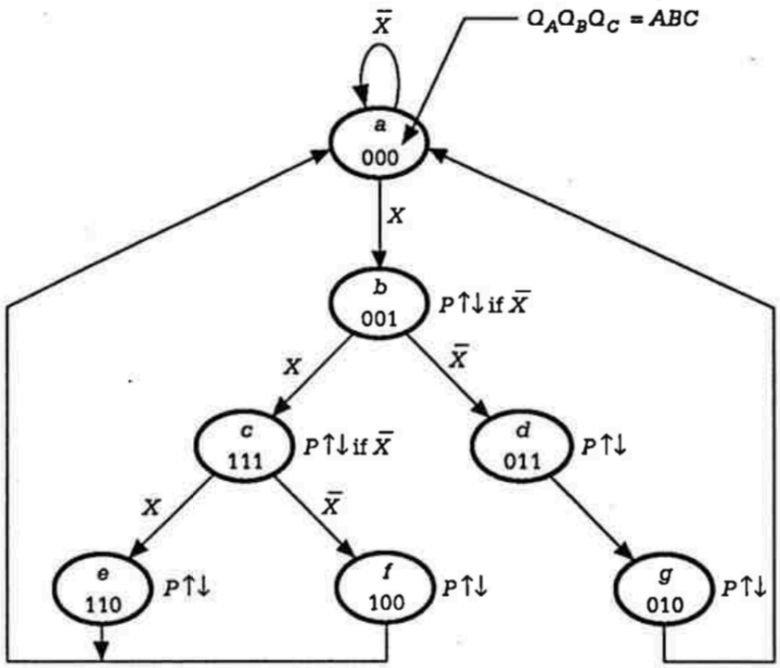
Once you have created, checked, and downloaded your design to the FPGA board, test it by toggling switch 0 and watching LED 0 toggle accordingly.

Task 2

Create a new project with a circuit that takes the 50Mhz clock as input and routes it directly to an output. Use A10 (*mclk*) as the input pin and A5 (*extout0*) as the output pin. Use the oscilloscope to verify that your circuit is working correctly by scoping the ***extout0*** pin on the FPGA board. Note that the purpose of this circuit is for you to know how to get the external clock (50 MHz) into the FPGA to use in future state machine designs.

Task 3

Create another new project by taking your circuit from Homework #5 (state diagram repeated at the right) and implementing it using the Xilinx FPGA. Use library parts such as D flip-flops, many types of AND, OR, NAND, etc. gates with various numbers of inputs, mux's, decoders, etc. Refer to the *Xilinx schematic library reference manual for ISE 14.7* handout posted to the class web page for details about each part in the Xilinx library. Note – use a negative edge-triggered D F/F for your state bits. I'll explain why later. Each lab group must use the following input and output pins on your FPGA boards:



Inputs

Flip-flop clock – sw9 (M9)
X – SW0 (P9)

Outputs

A – led0 (L14)
B – led1 (L16)
C – led2 (K16)
P – led3 (K15)

Have the instructor or lab TA check out your design and operation.

To Turn In

By next lab period, a team created short report containing:

- Abstract (a concise and to the point description of what was accomplished);
- Block diagram;
- Schematic - print-out from Xilinx (if the printer is working 😩);
- Summary statement giving results achieved, discussion of any problems encountered, design notes, and anything else you wish to include;
- Note – each person needs to turn in a report but you may copy the needed information from your lab partner.