Engr433 Lab #6

VHDL Implementation Using an FPGA – Advanced

Name _____

Partner _____ Grade _____/10

Objective

Continue learning VHDL by designing and implementing a circuit containing both combinational and sequential logic circuits.

References

- This handout;
- Xilinx documents on the class web page including *VHDL Entry Using ISE 14.7 Tutorial*

Design Flow

- Initial design (block diagram in particular);
- Describe the design using VHDL;
- Synthesize using Xilinx software;
- Download to FPGA board using Impact;
- Test with oscilloscope.

Task

- Design a logic circuit that will create the set of waveforms shown in Figure1. The "clock" shown in Figure1 is a derived clock, not 50Mhz, whose rate can be selected as either 50Khz or 5Khz. Rate will be selected with a button in a push-on, push-off way that toggles between the two rates (see the example state diagram in Figure 2). For this lab, ignore potential switch bounce.
- The 50Mhz master clock, derived clock, and four waveform signals (sync, data1, data2, data3) are all to be routed to FPGA output pins (see definition on the next page). Make other signals visible at your own discretion. This is to allow observation of the waveforms with an oscilloscope.
- Please don't use code from previous years students. Make every effort to aid your own understanding of VHDL by writing original code.

Initial Design

Before writing any VHDL, create a neat block diagram (pencil/paper or electronic tool) showing the circuit functional blocks you need to create, and the interconnections between them. When writing the VHDL description for this block diagram you should be able to easily identify the statements that relate to each block (i.e. put in comments) but you don't have to create separate entities/architectures with structural instantiation. You can have one entity for the overall design and one architecture with multiple processes and assignment statements (with appropriate comments) that reflect the function of each block in the block diagram. Show the lab instructor your block diagram before proceeding to VHDL.

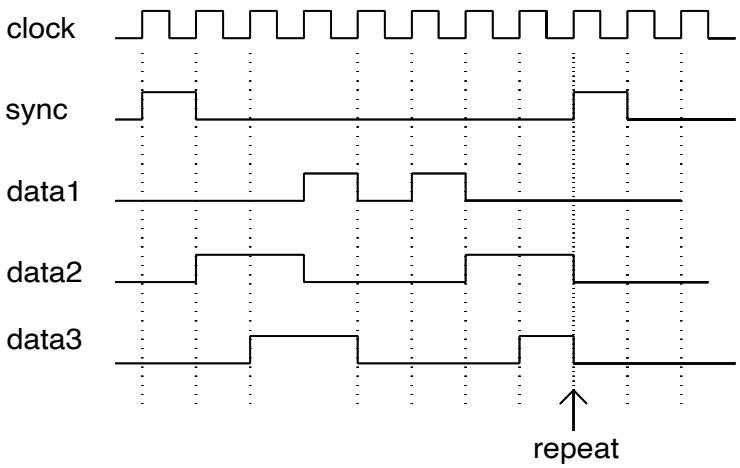

Figure 1

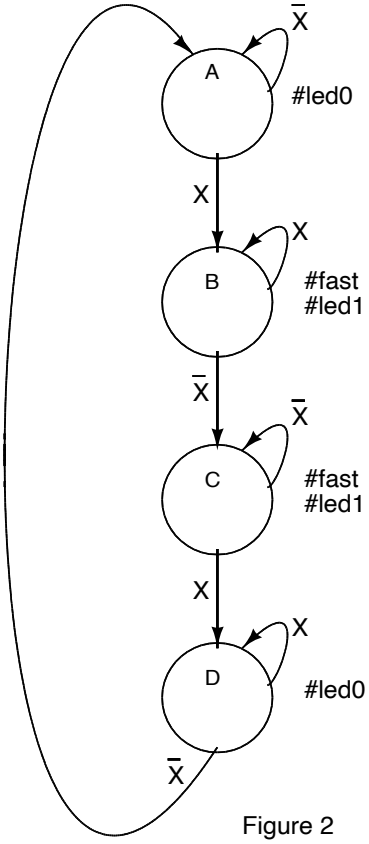

Figure 2

FPGA Pinout Definition

Input Connections

Master clock (50Mhz)	mclk	A10
Rate select switch	sw8	M9

Output Connections

Master clock (50Mhz)	extout8	A9
Derived clock	extout4	A7
Sync	extout0	A5
Data1	extout1	B6
Data2	extout2	A6
Data3	extout3	C7

To Turn In

A report is required from each person and consists of:

- A one-page synopsis of what you did in lab, procedures followed, results, and problems if any.
- Block diagram.
- Hardcopy of the VHDL file you create.
- Statistics including number of slice F/Flops used, # of occupied slices, # of slices containing unrelated logic, number of bonded IOBs, the number of BUFGMUXs, and average fanout of non-clock nets.
- If you worked with a partner list your partners name.