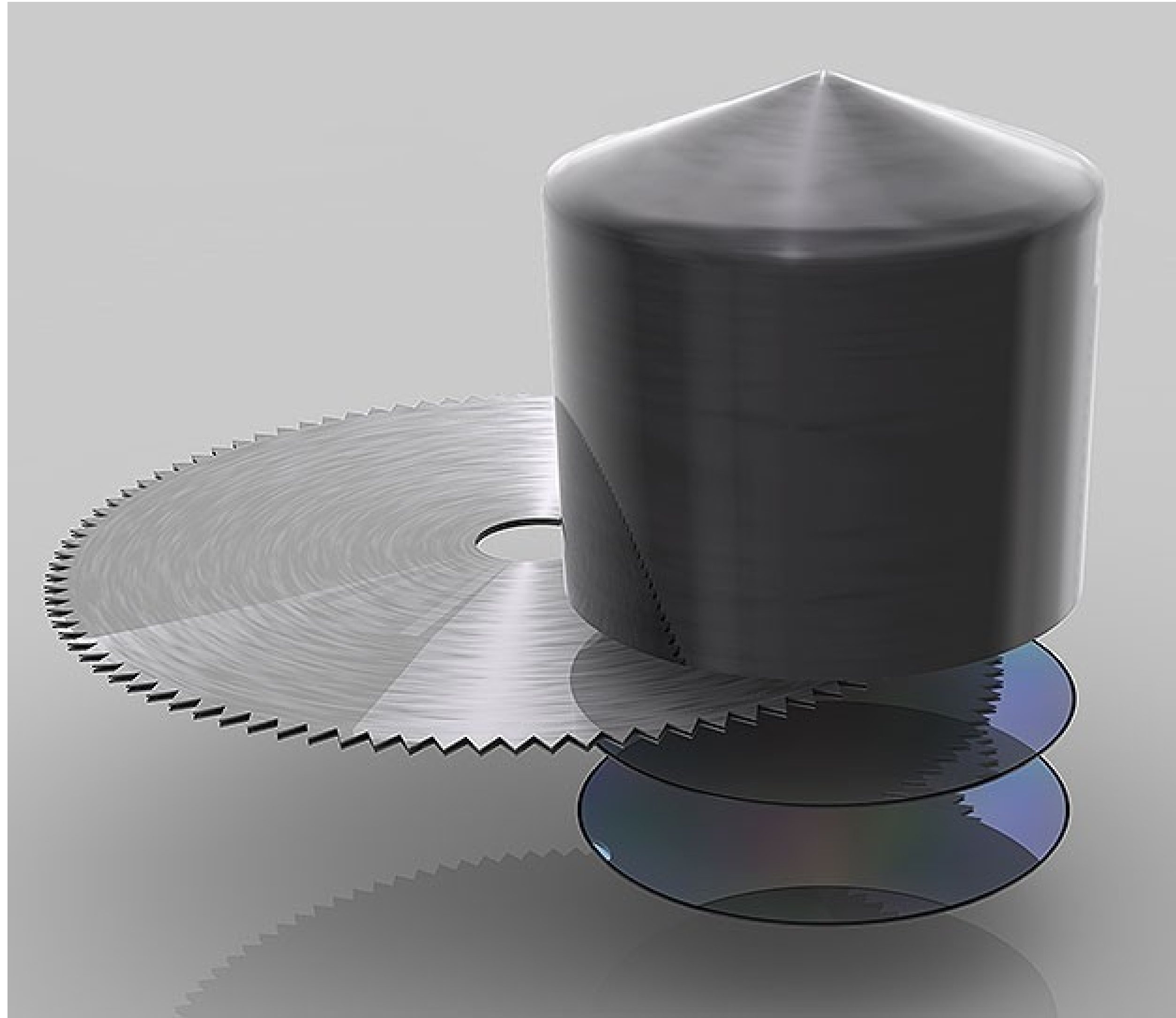
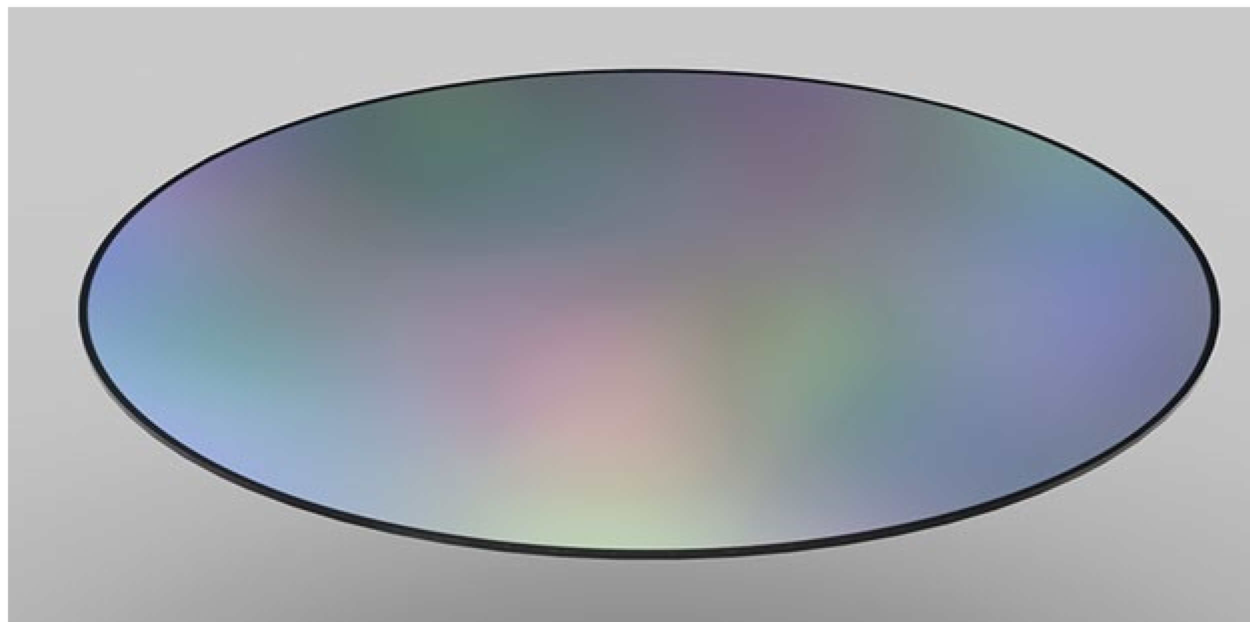
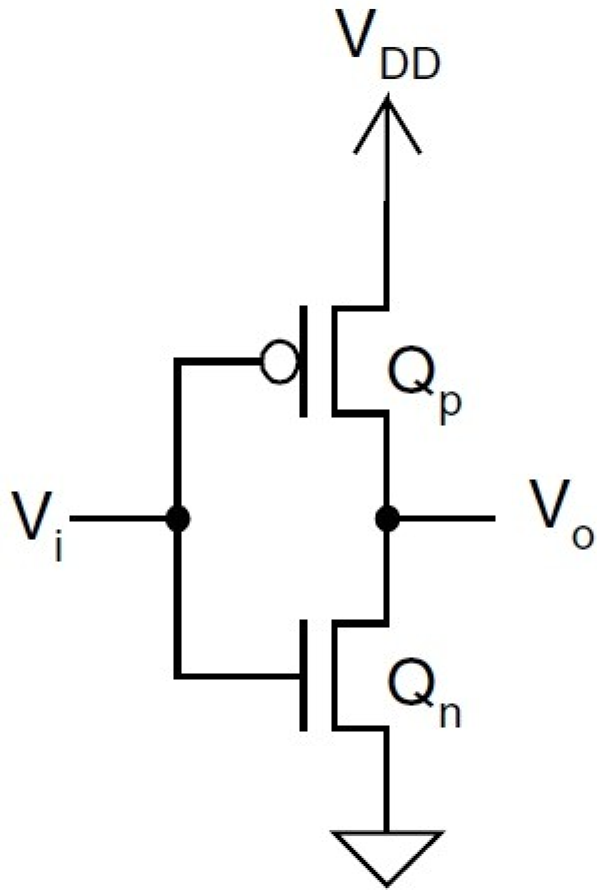
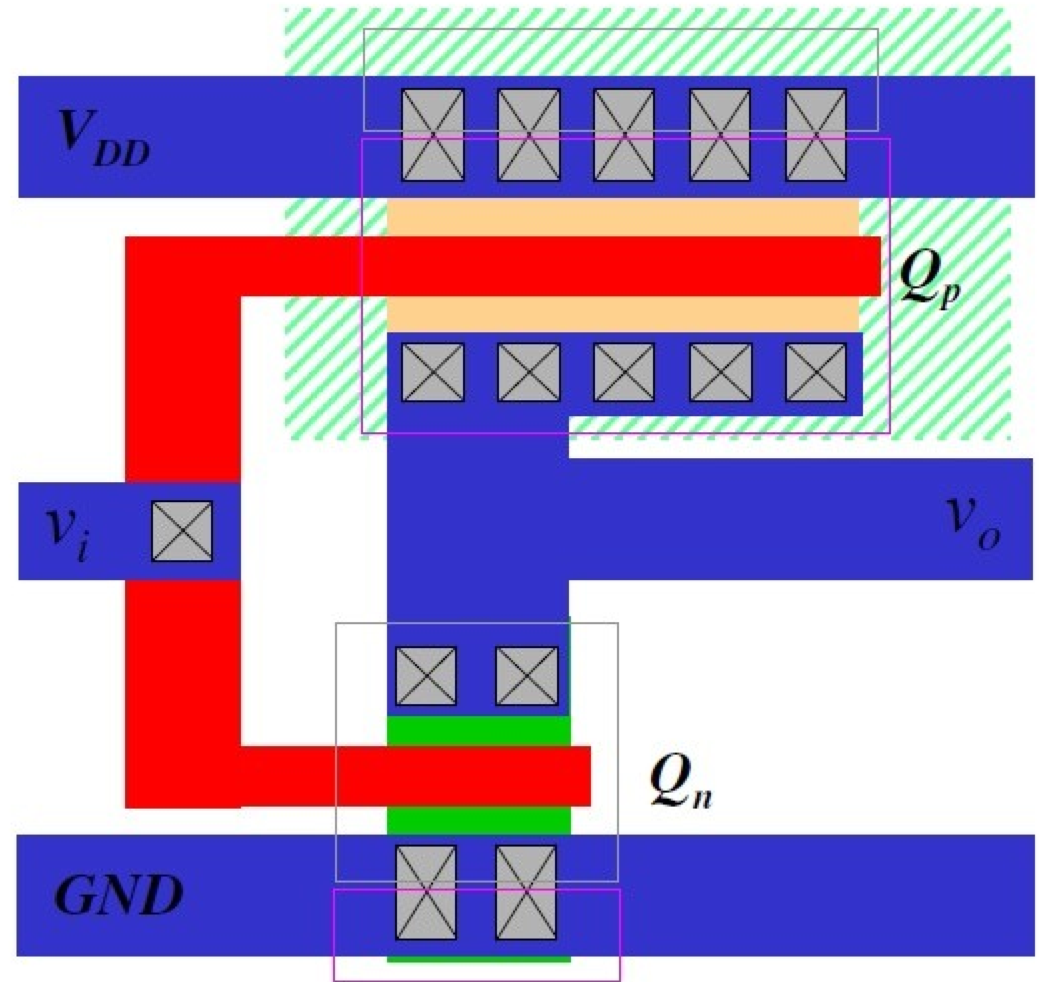
IC Fabrication

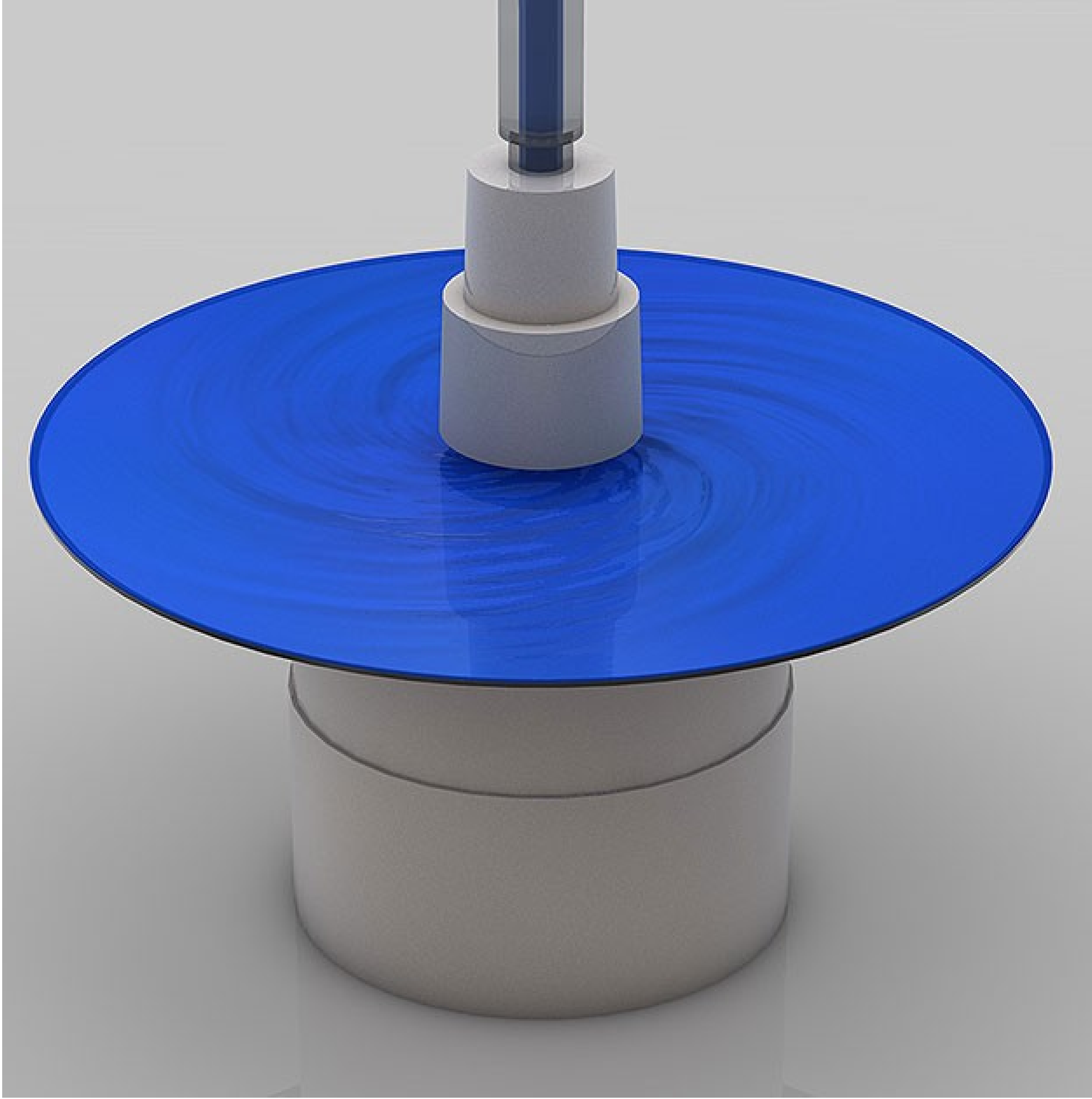


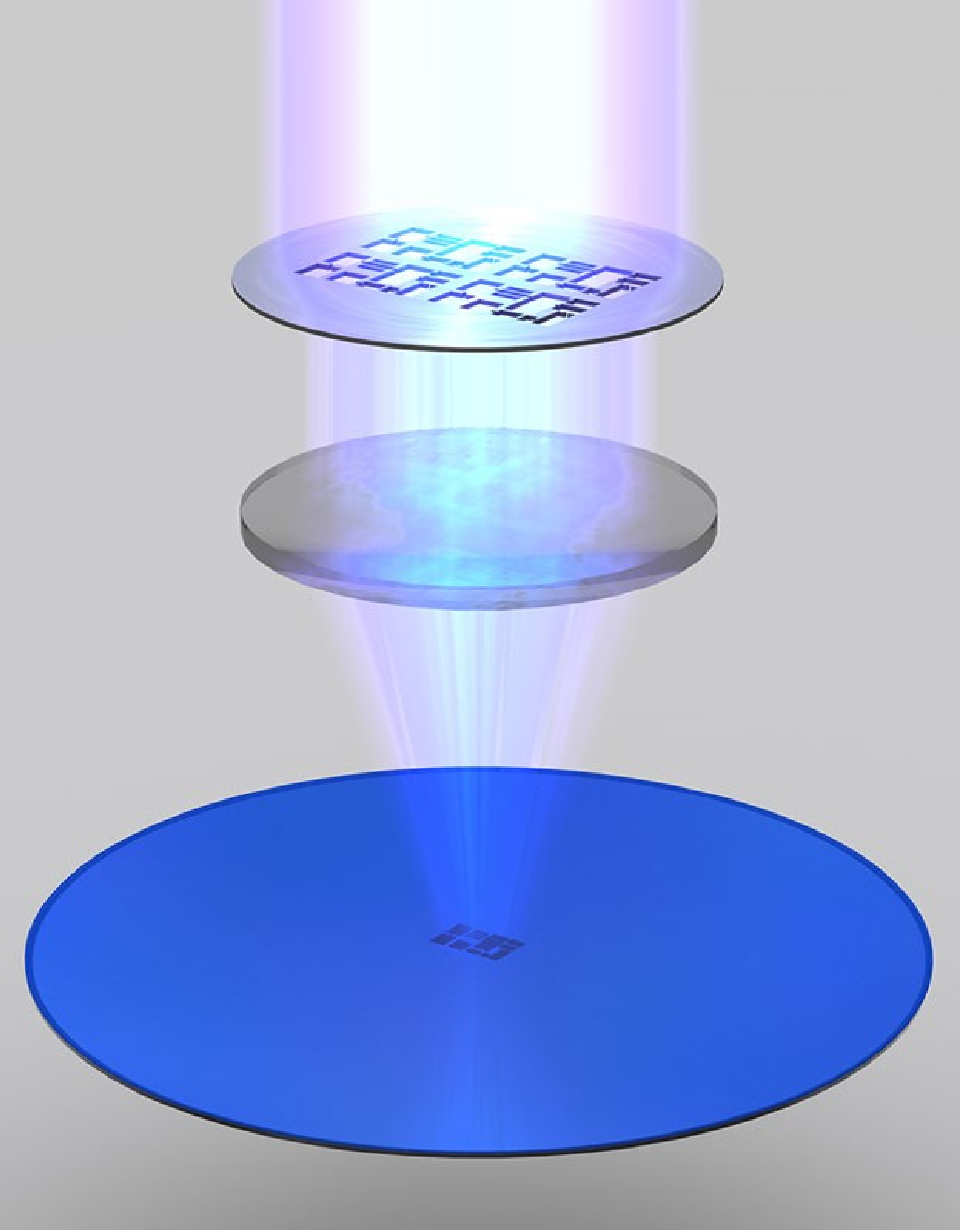


CMOS Inverter



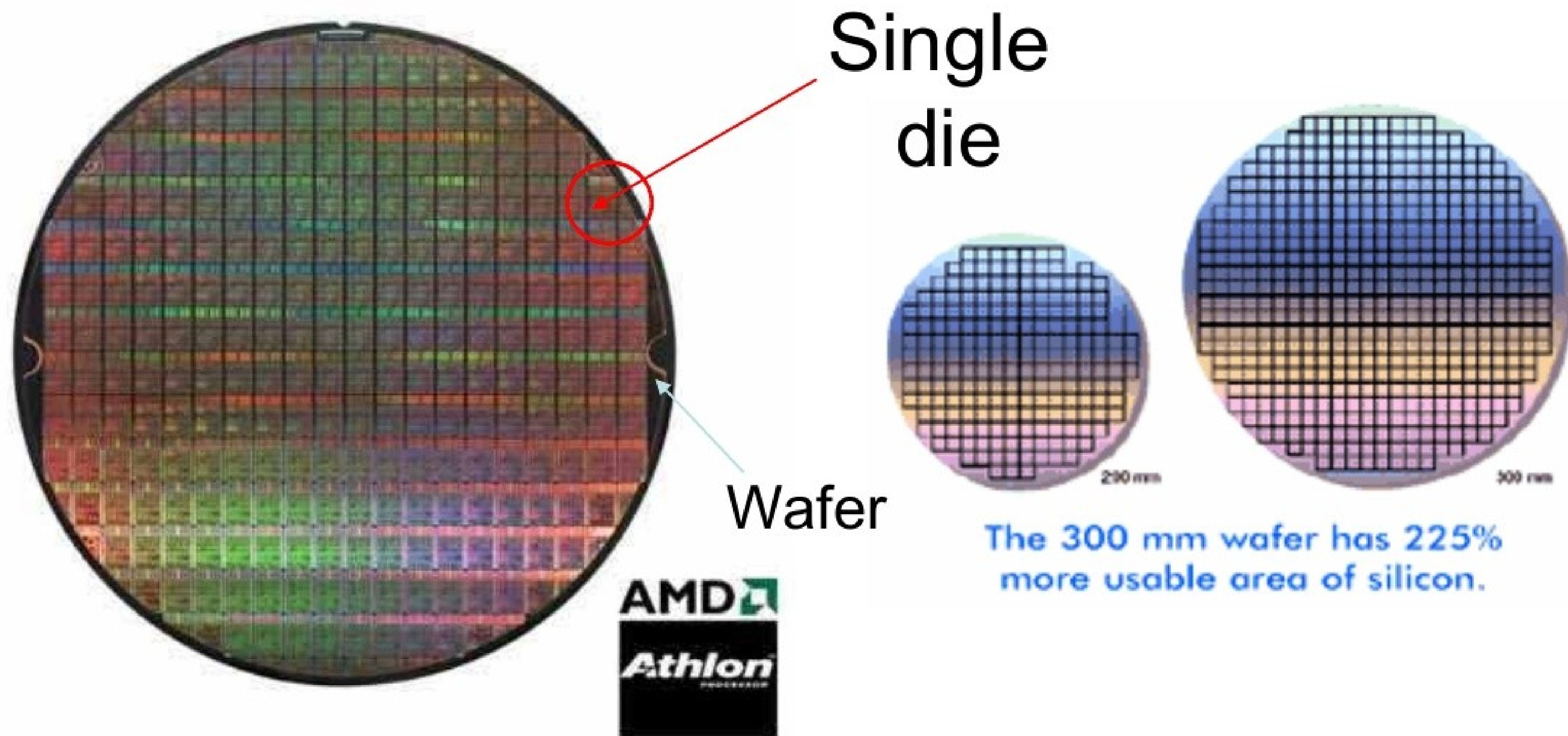






晶片的大小

- 晶圓的照片（Wafer photo）

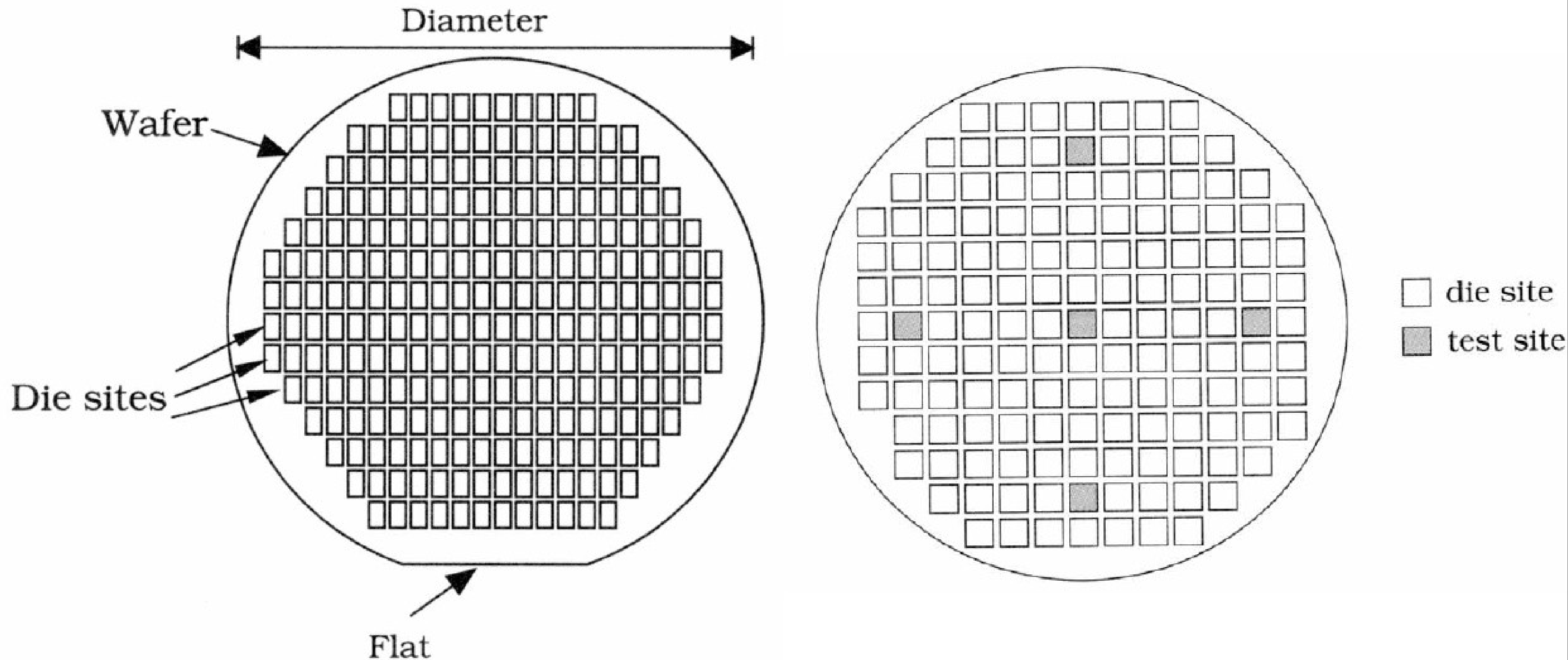


From http:/ / www.amd.com

已提昇至 12” (30cm)

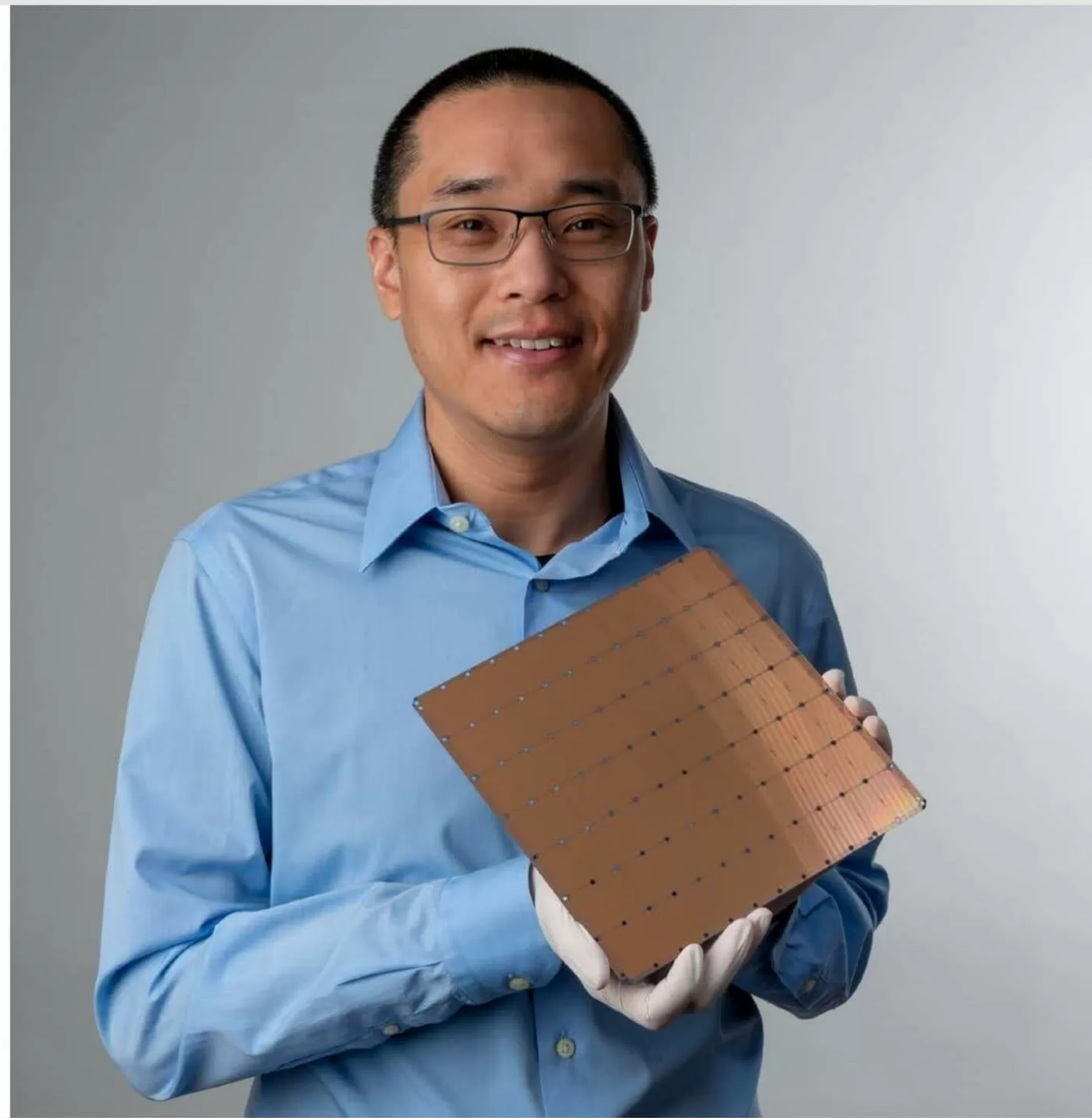
Wafer, Die, and IC

- Yield
- Defect density

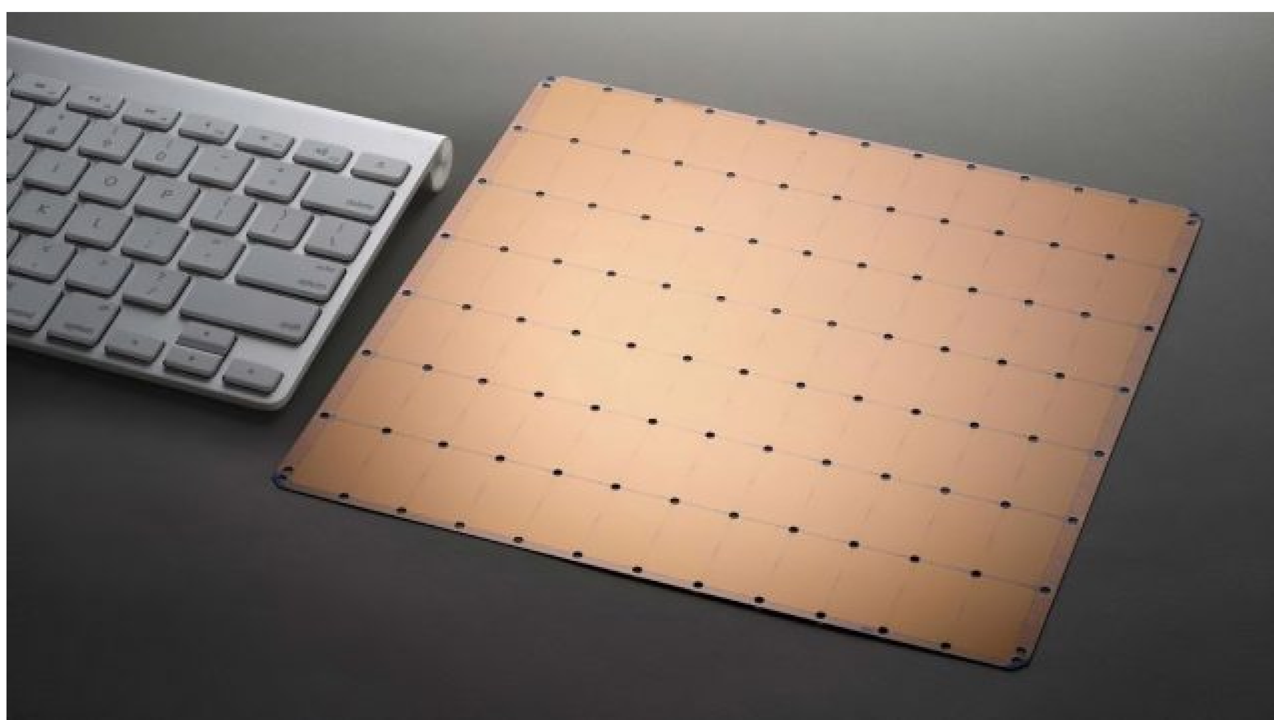


Largest Chip Ever Built

- 46,225 mm^2 silicon
- 1.2 trillion transistors
- 400,000 AI optimized cores
- 18 Gigabytes of On-chip Memory
- 9 PByte/s memory bandwidth
- 100 Pbit/s fabric bandwidth
- TSMC 16nm process



cerebras



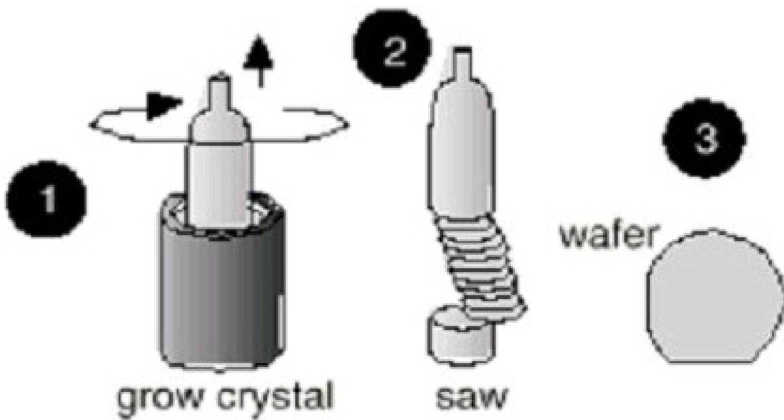
Wafer Scale Engine – Generation 2

850,000 **AI-optimized cores**

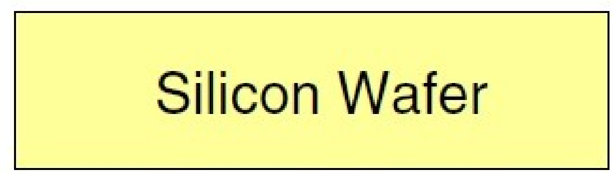
2.6 Trillion **Transistors**

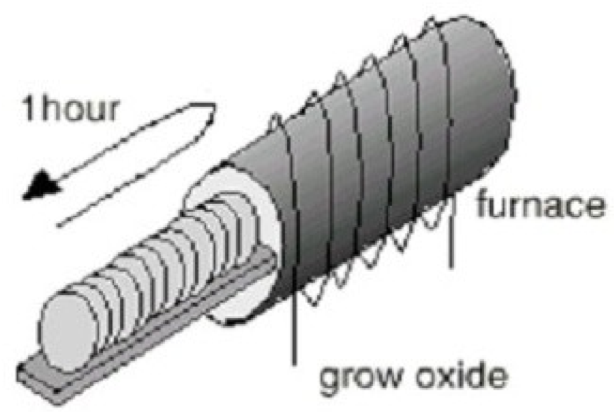
TSMC 7nm **Process**

The CMOS process -> Photolithography

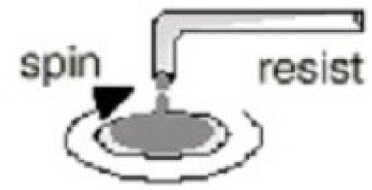


(a) Bare silicon wafer

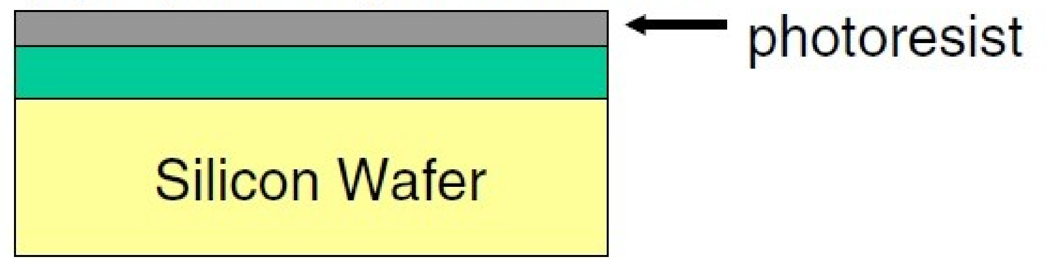




(b) Grow Oxide layer

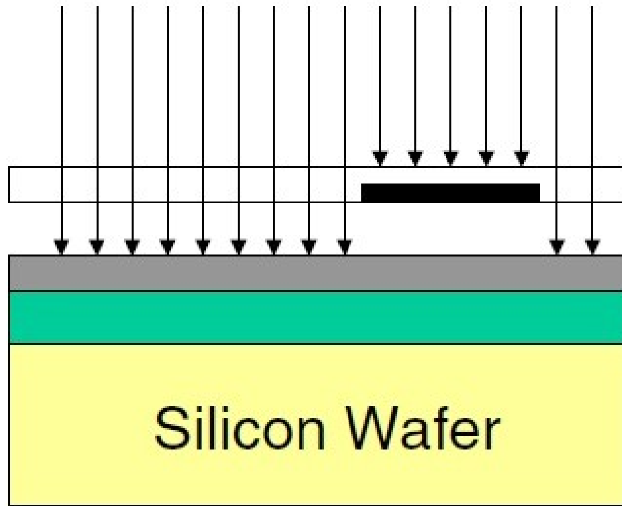


(c) Spin on photoresist



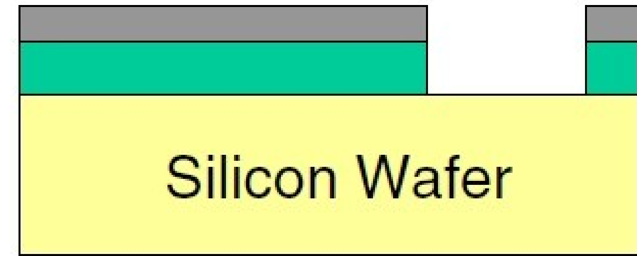
Photolithography - continued

(d) Expose resist to UV light through a MASK



(e) Remove unexposed resist

(f) Etch away oxide



(g) Remove remaining resist

Silicon Dioxide (SiO_2)

- Thin oxide, using dry oxidation
  - Material under the gate terminal of MOS
- Thick oxide (field oxide), using wet oxidation
  - Isolation between MOS
- CVD (chemical vapor deposition) oxide
  - Isolation between layers

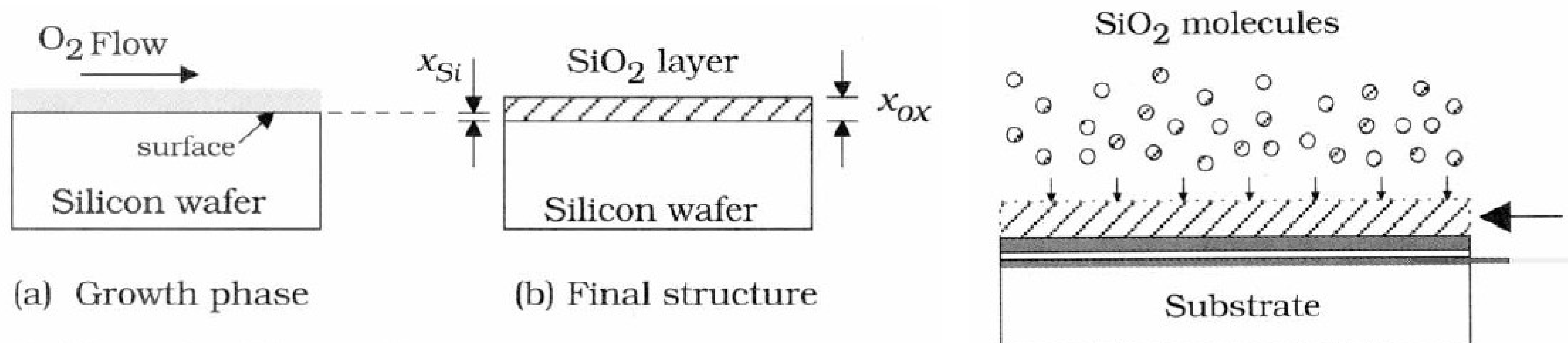
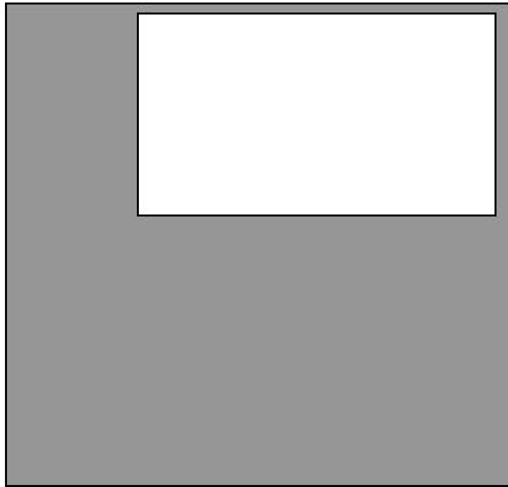


Figure 4.2 Thermal oxide growth

Mask 1 : N-well Diffusion

- *SiO_2* is etched using *Mask 1.*



- *Phosphorous is diffused into the unmasked regions of silicon creating an n-well for the fabrication of p-channel devices*

Phosphorous Diffusion

SiO_2

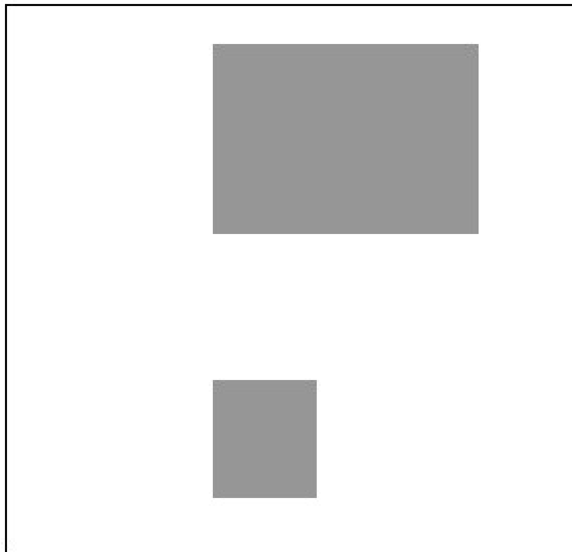
p-substrate

n-well

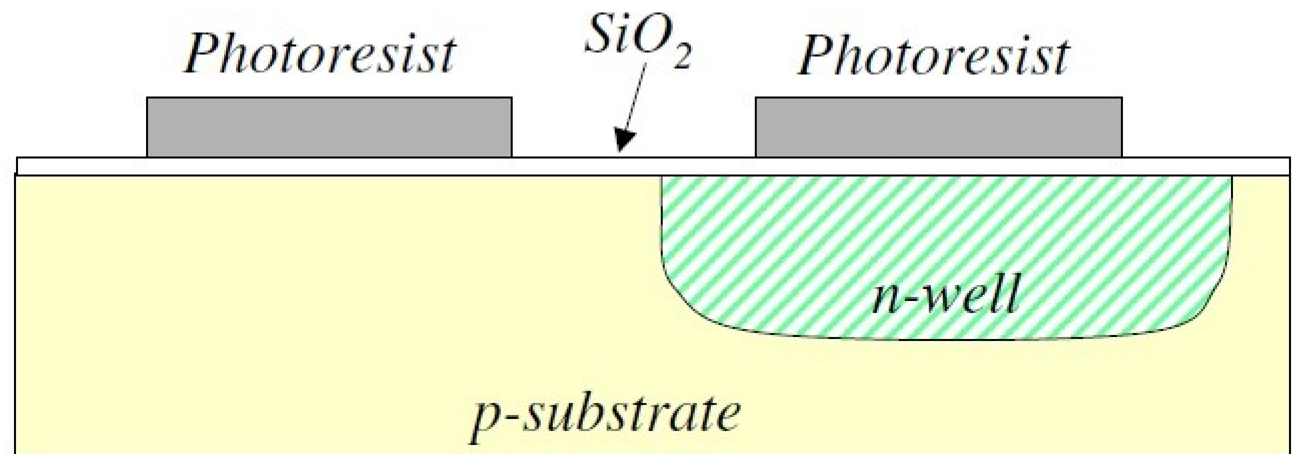
p-substrate

Mask 2 : Define Active Regions

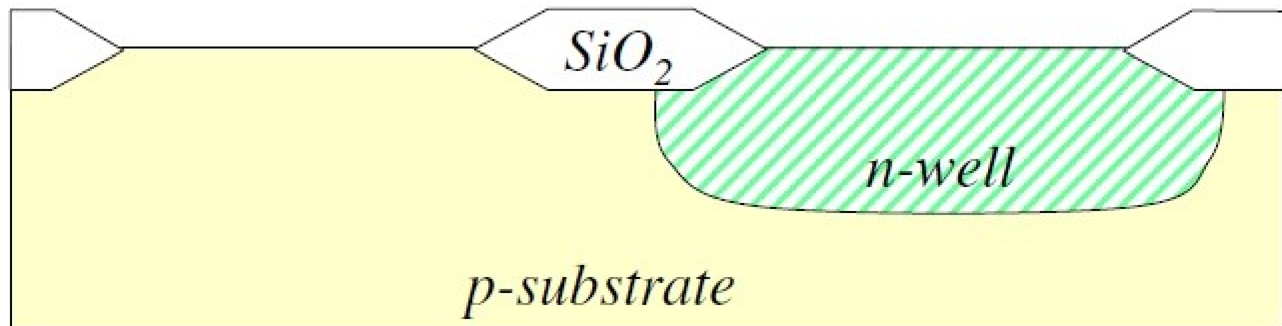
- *Mask 2 creates the active regions where the MOSFETs will be placed*



- *The thick oxide regions provides isolation between the MOSFETs*

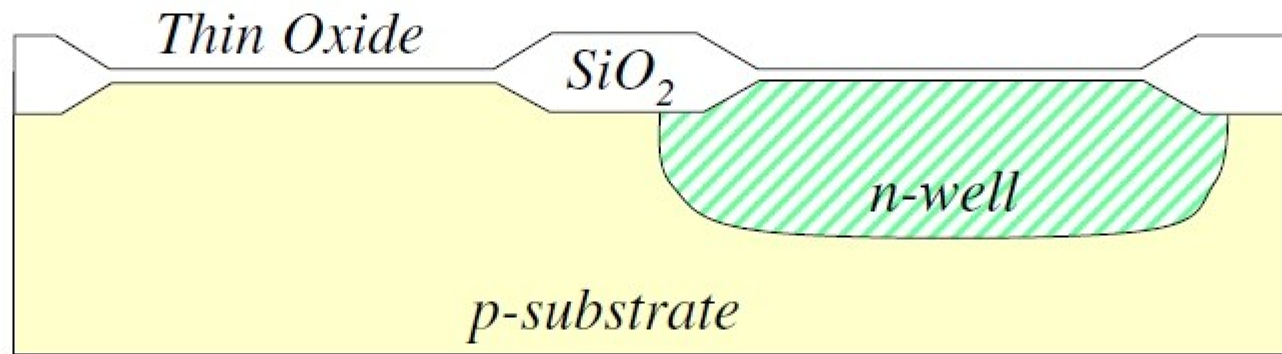


A thick field oxide is grown using a contruction technique called Local Oxidation Of Silicon (LOCOS).

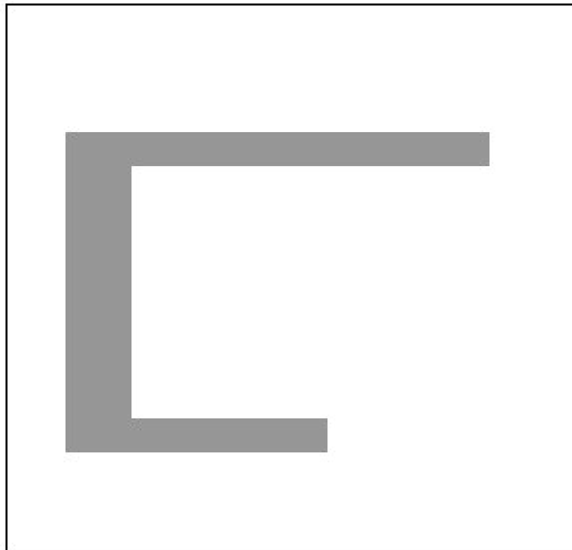


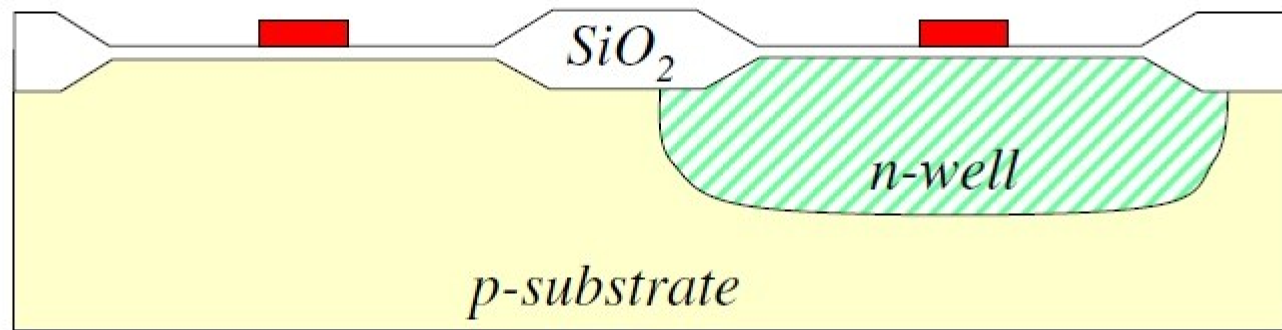
Mask 3 : Polysilicon Gate

- A high quality thin oxide is grown in the active area *(~100 ->300)*
- *Mask 3* is used to deposit the polysilicon gate *(most critical step)*



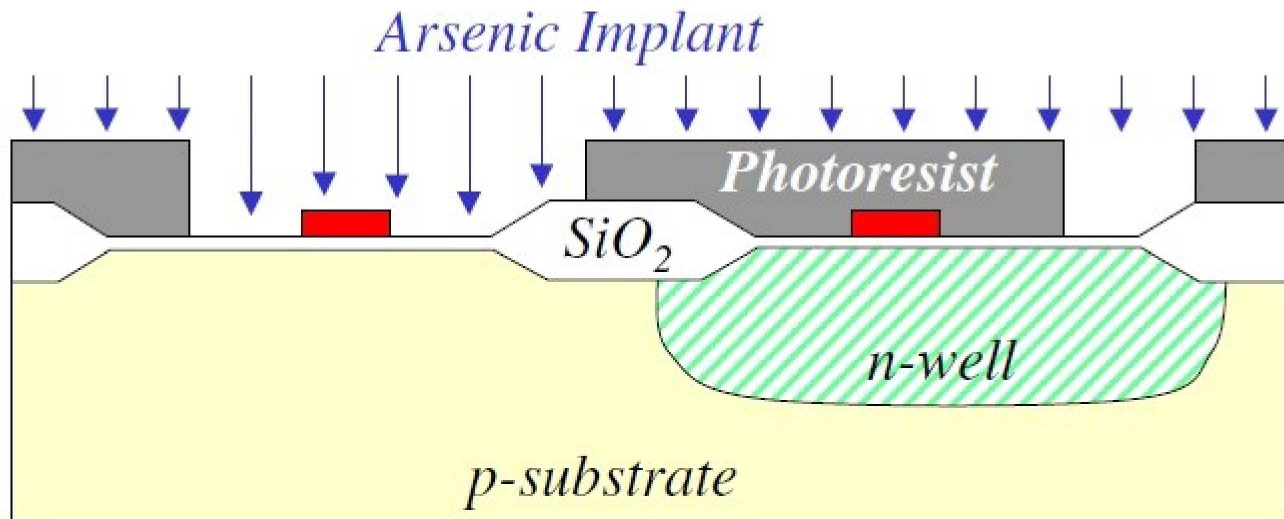
The polysilicon layer is usually arsenic doped (n-type). The photolithography in this step is the most demanding since it requires the finest resolution to create the narrow MOS channels.

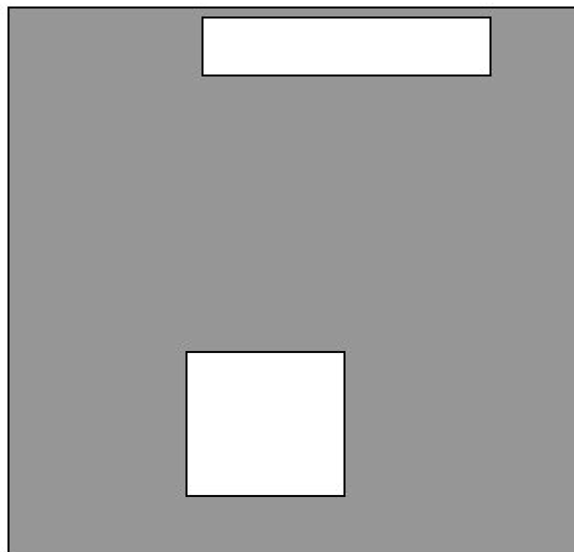




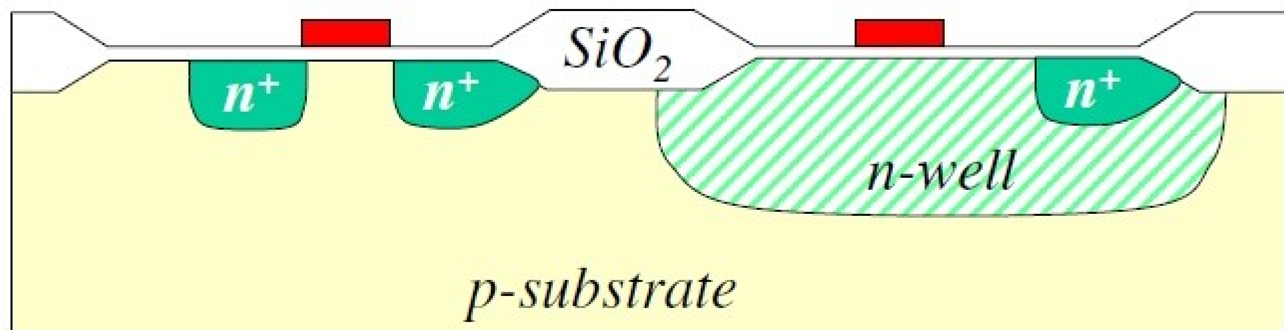
Mask 4 : n+ Diffusion

- *Mask 4* is used to control a heavy arsenic implant and create the source and drain of the n-channel devices.
- This is a **self-aligned** structure.



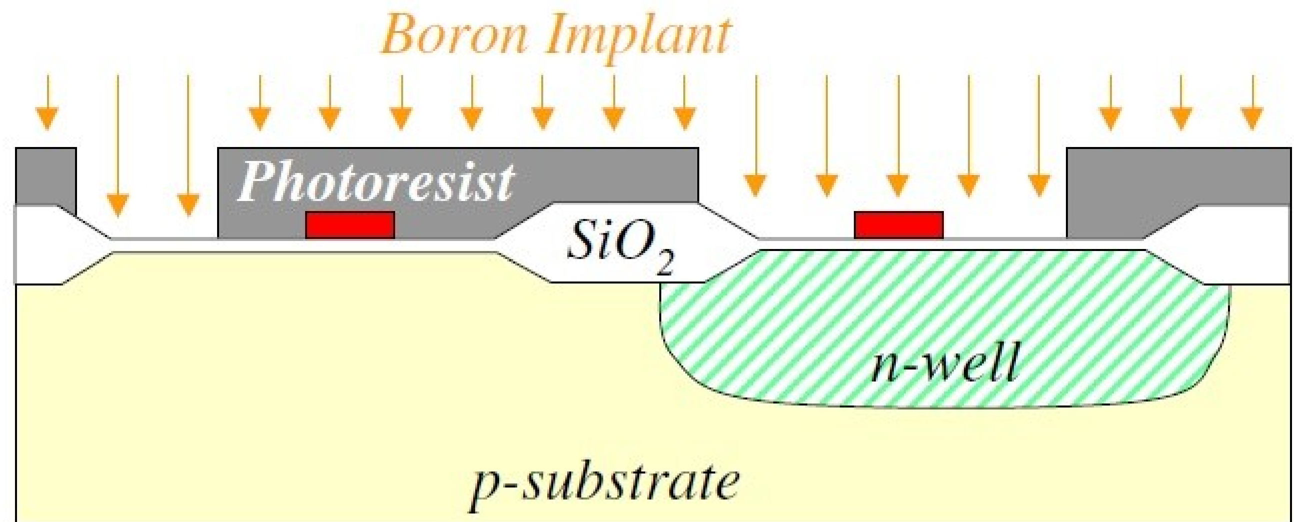


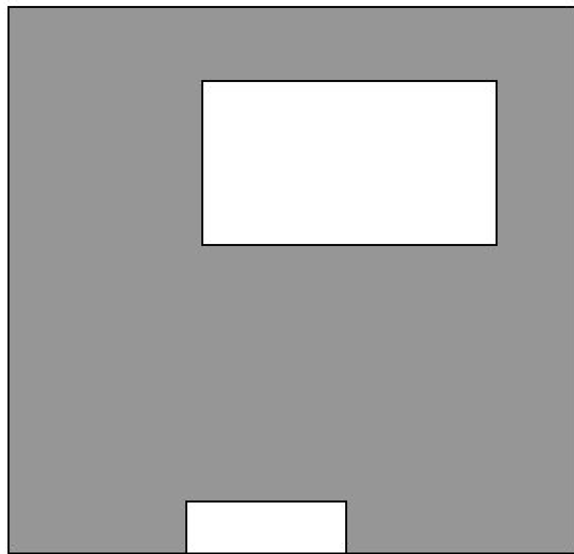
The polysilicon gate acts like a barrier for this implant to protect the channel region.



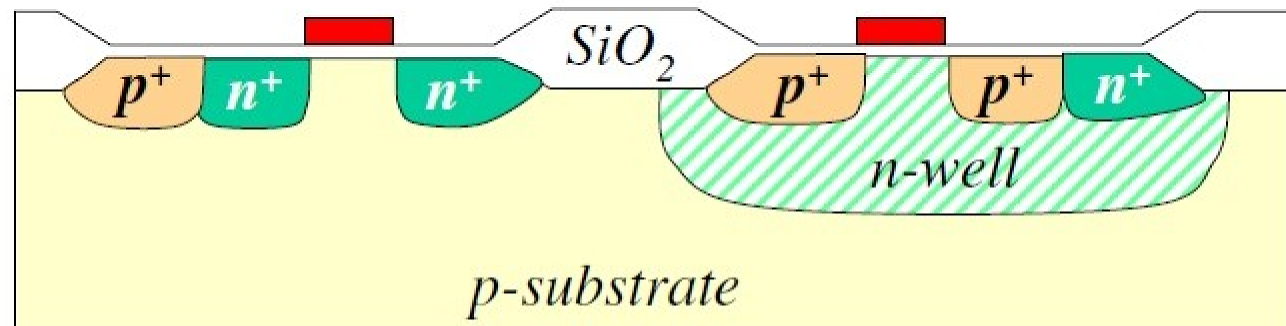
Mask 5 - p+ diffusion

- *Mask 5* is used to control a heavy Boron implant and create the source and drain of the n-channel devices.
- This is a self-aligned structure.



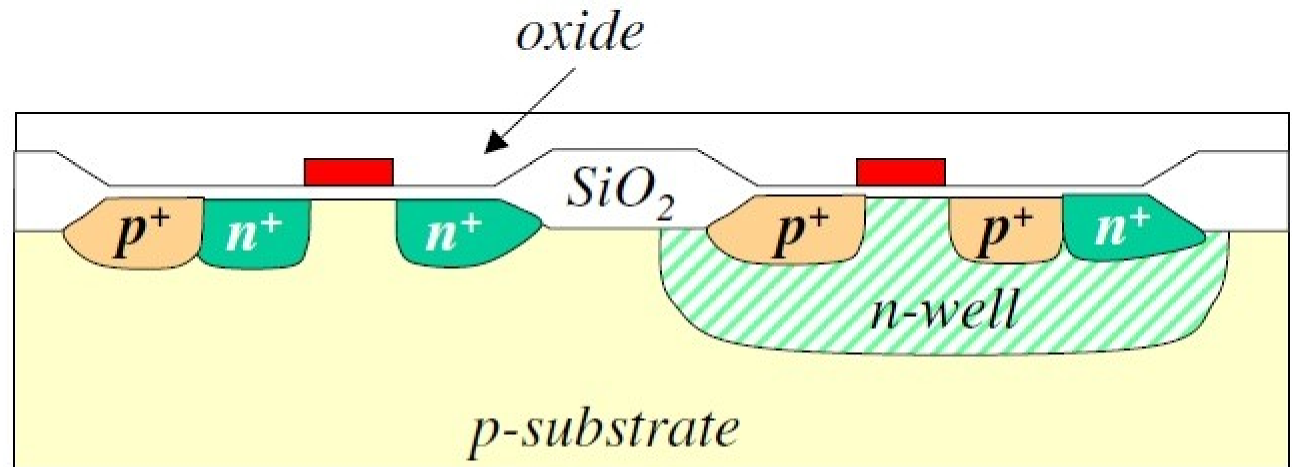


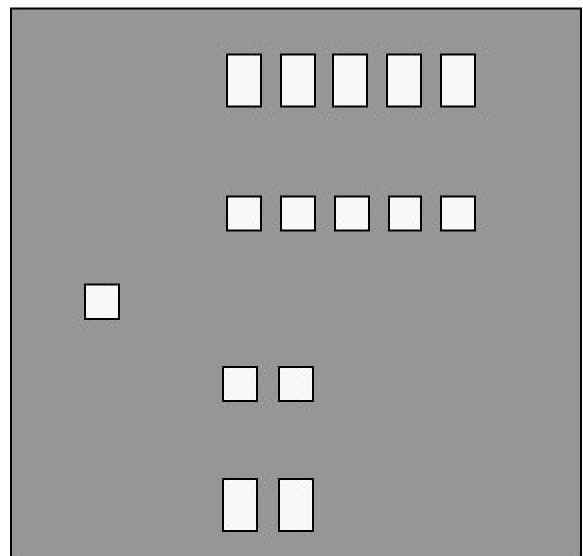
The polysilicon gate acts like a barrier for this implant to protect the channel region.

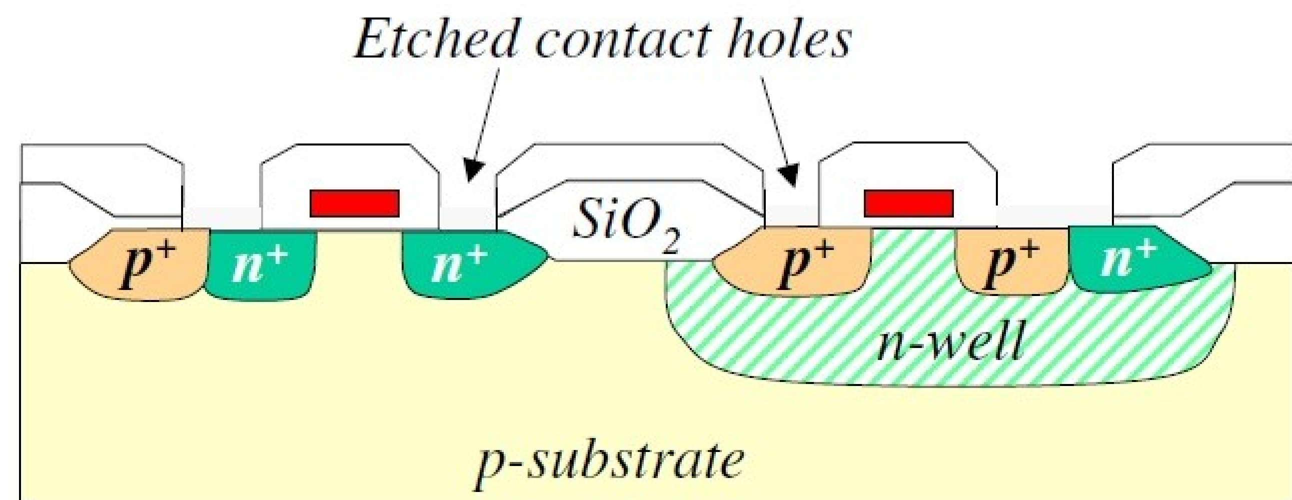


Mask 6 - Contact Holes

- A thin layer of oxide is deposited over the entire wafer
- *Mask 6* is used to pattern the contact holes
- Etching opens the holes.

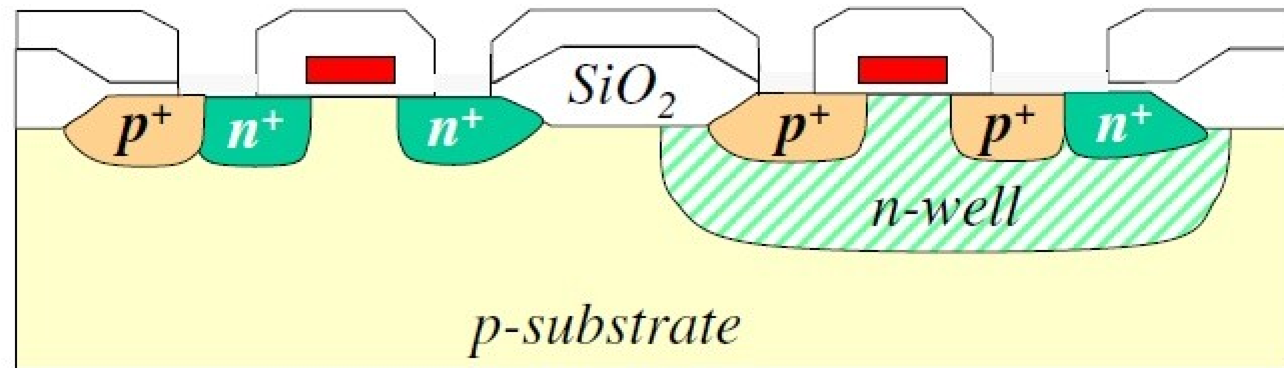


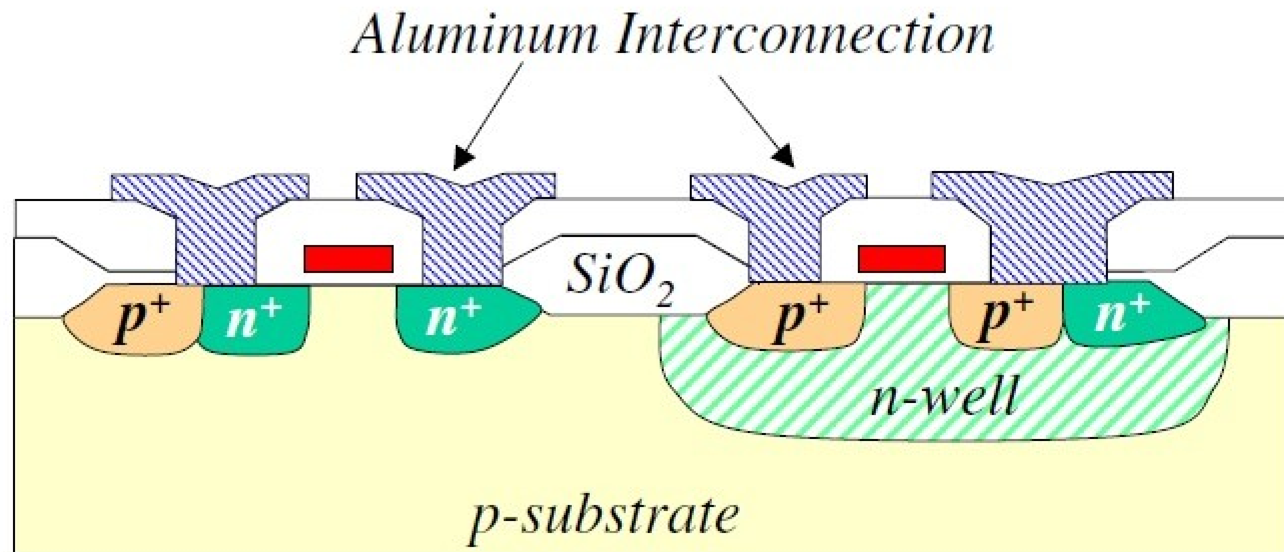




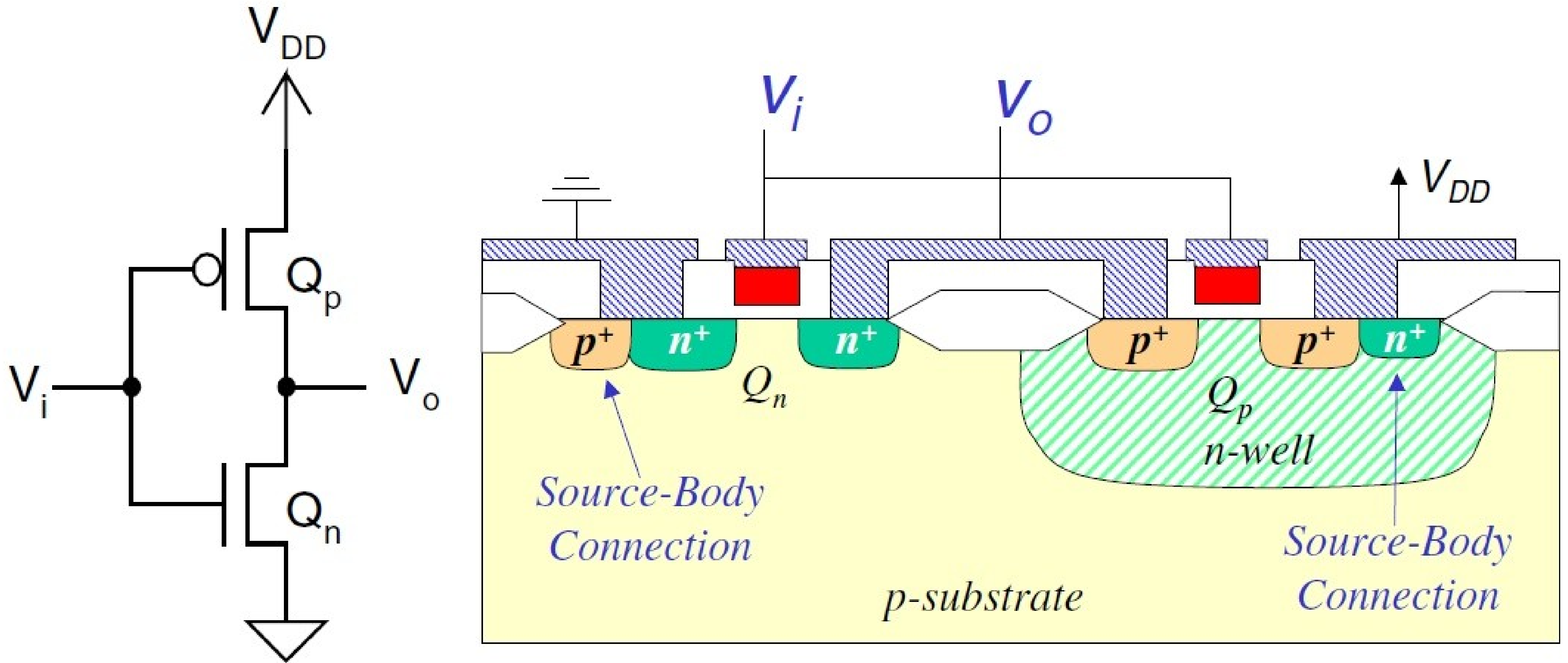
Mask 7 : Metalization

- A thin layer of aluminum is evaporated or sputtered onto the wafer.
- *Mask 7* is used to pattern the interconnection.



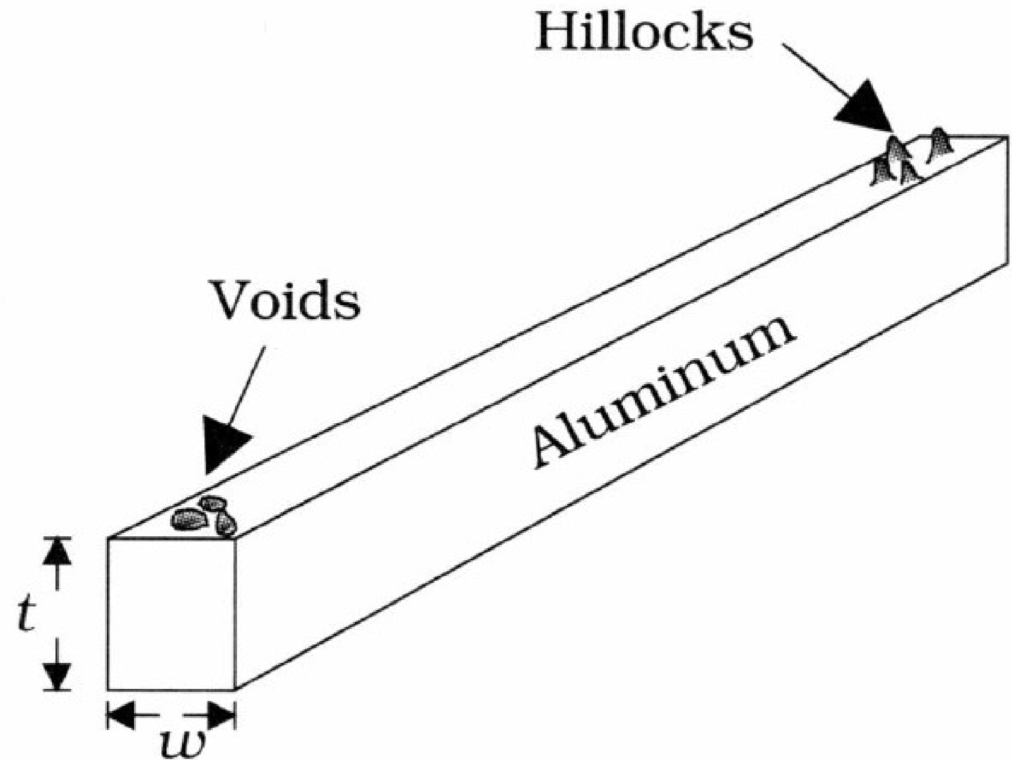


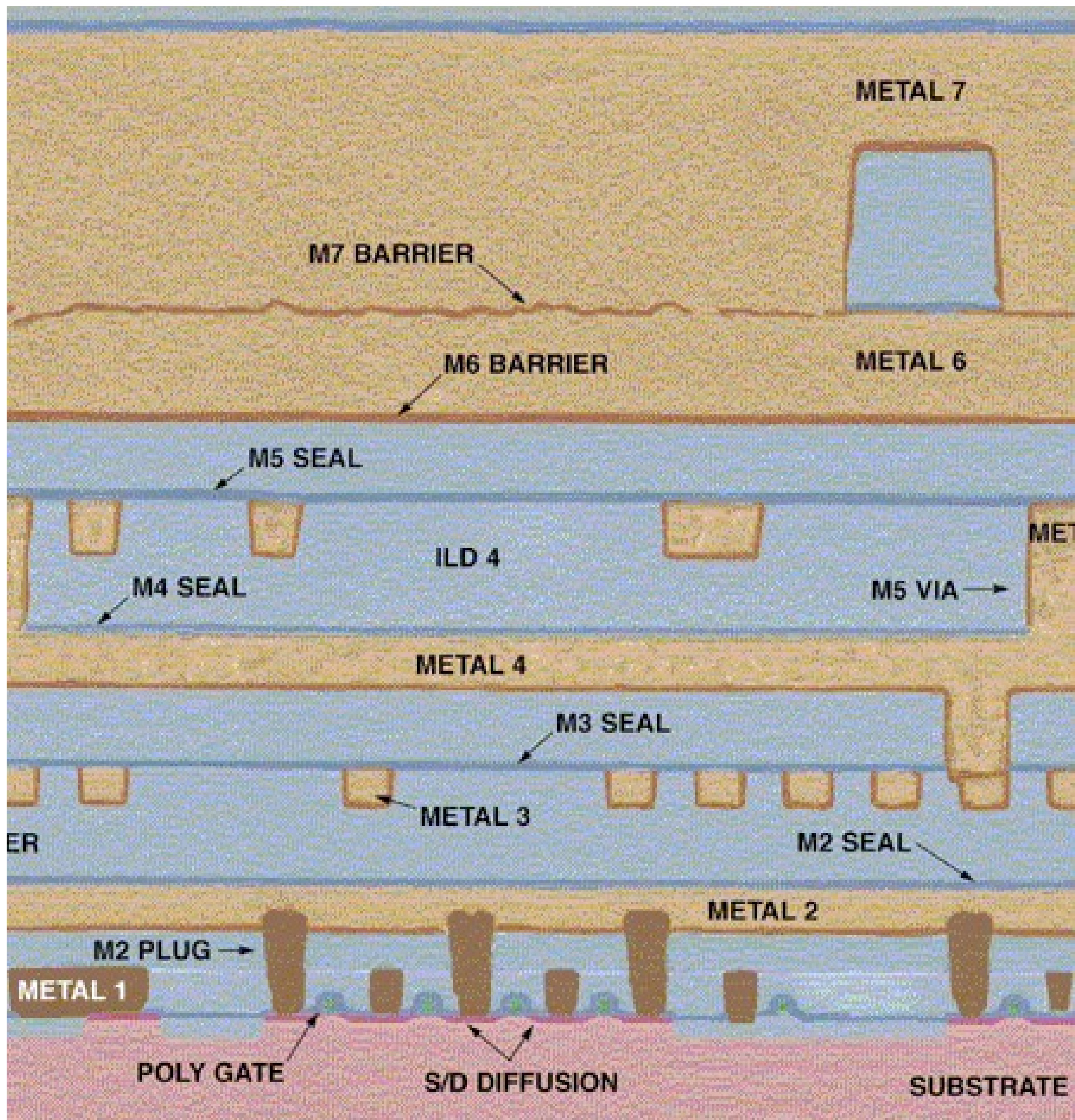
Cross section of the CMOS inverter

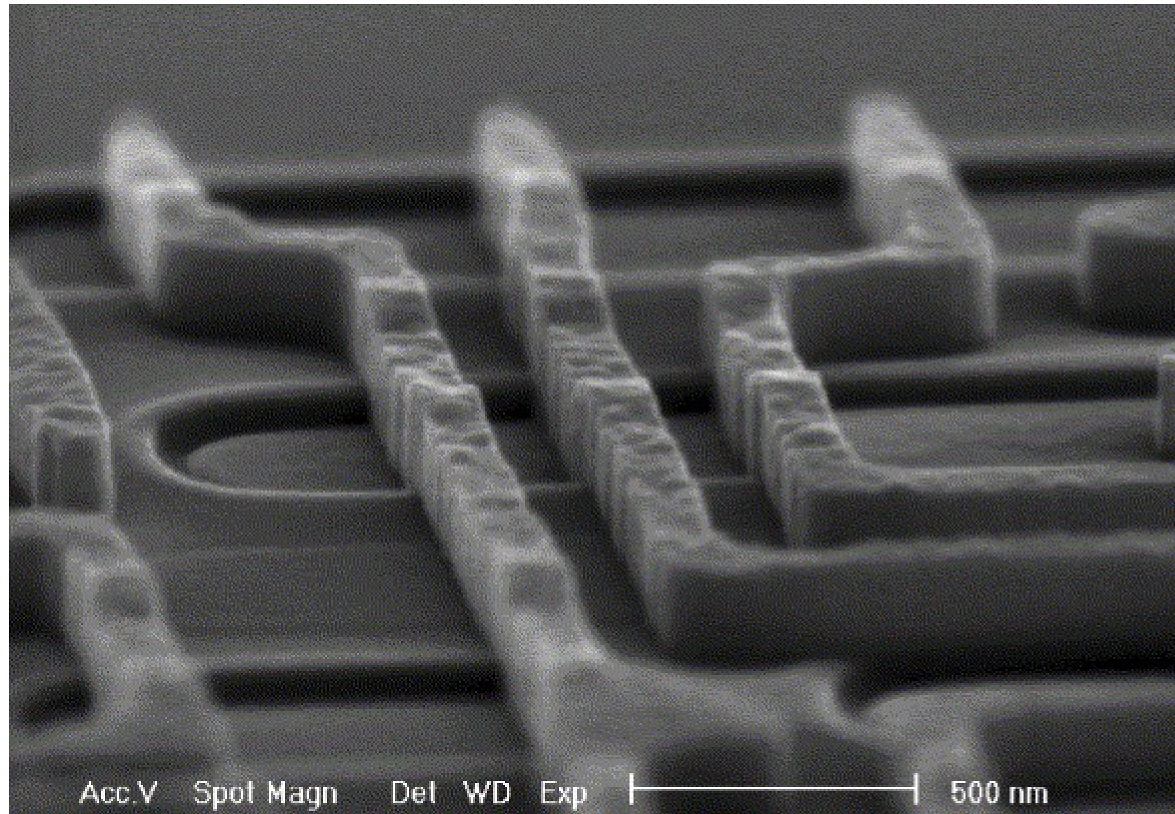


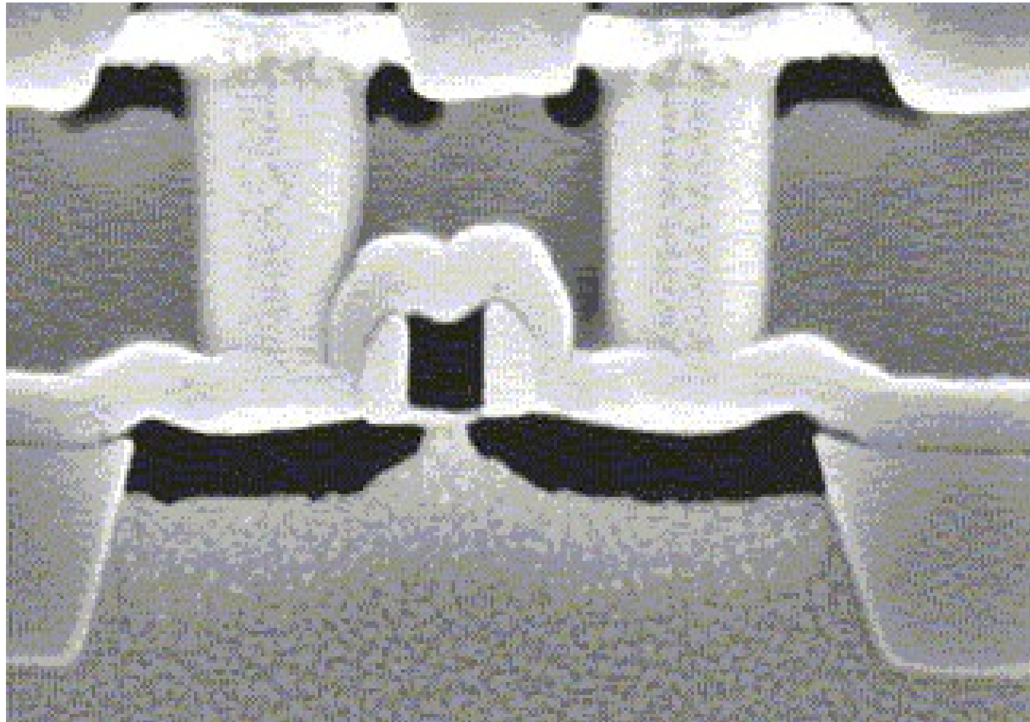
Metal

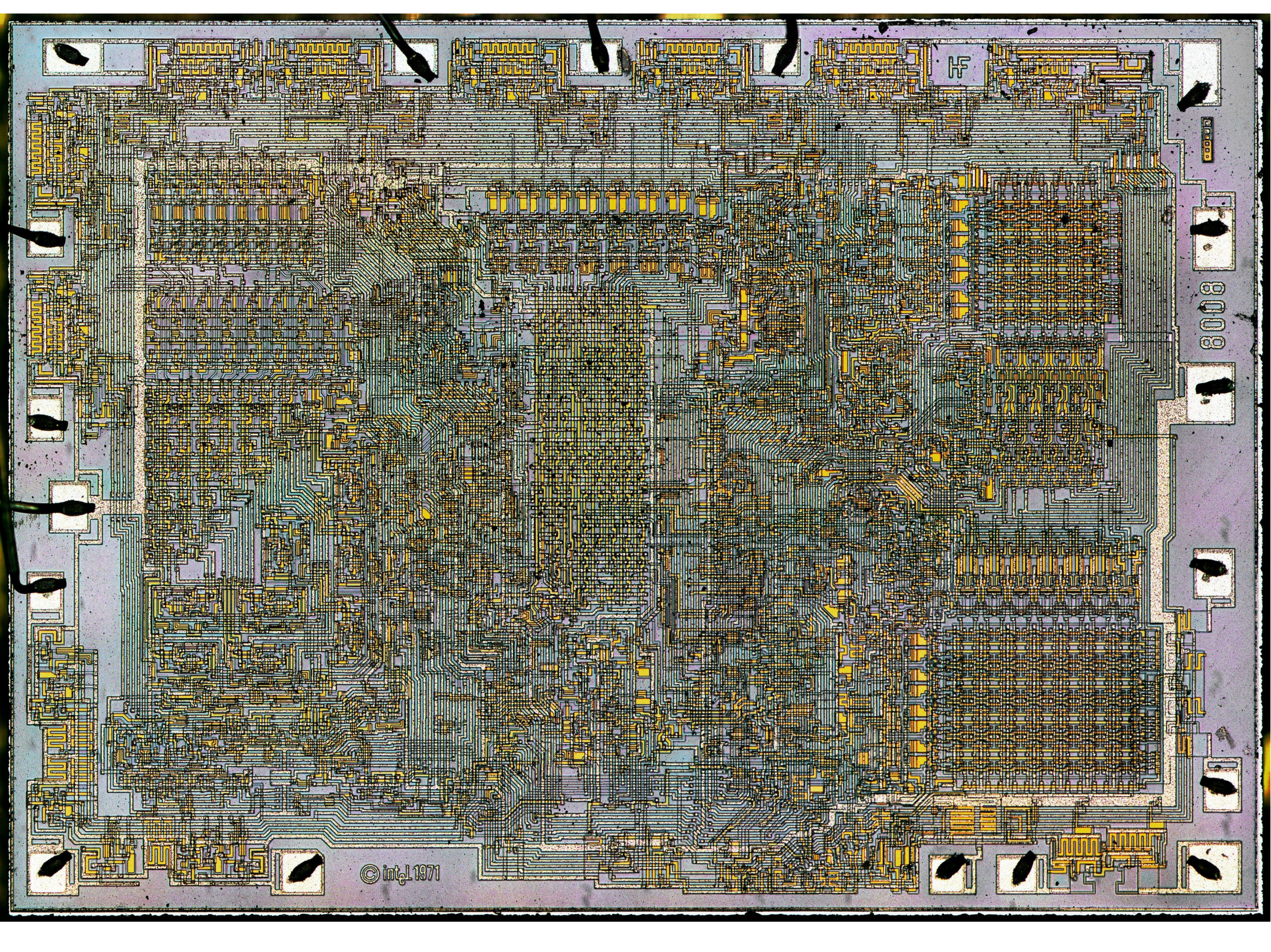
- Aluminum (Al)
  - Material or metal layers
  - Suffers electromigration
- Copper
  - Half resistance of Al
  - Much harder process




METAL 7
M7 BARRIER
M6 BARRIER
METAL 6
M5 SEAL
ILD 4
M4 SEAL
M5 VIA
METAL 4
M3 SEAL
METAL 3
M2 SEAL
METAL 2
M2 PLUG
METAL 1
POLY GATE
S/D DIFFUSION
SUBSTRATE


Acc.V Spot Magn Det WD Exp
500 nm




HF
8008
© intel 1971

Bonding pad

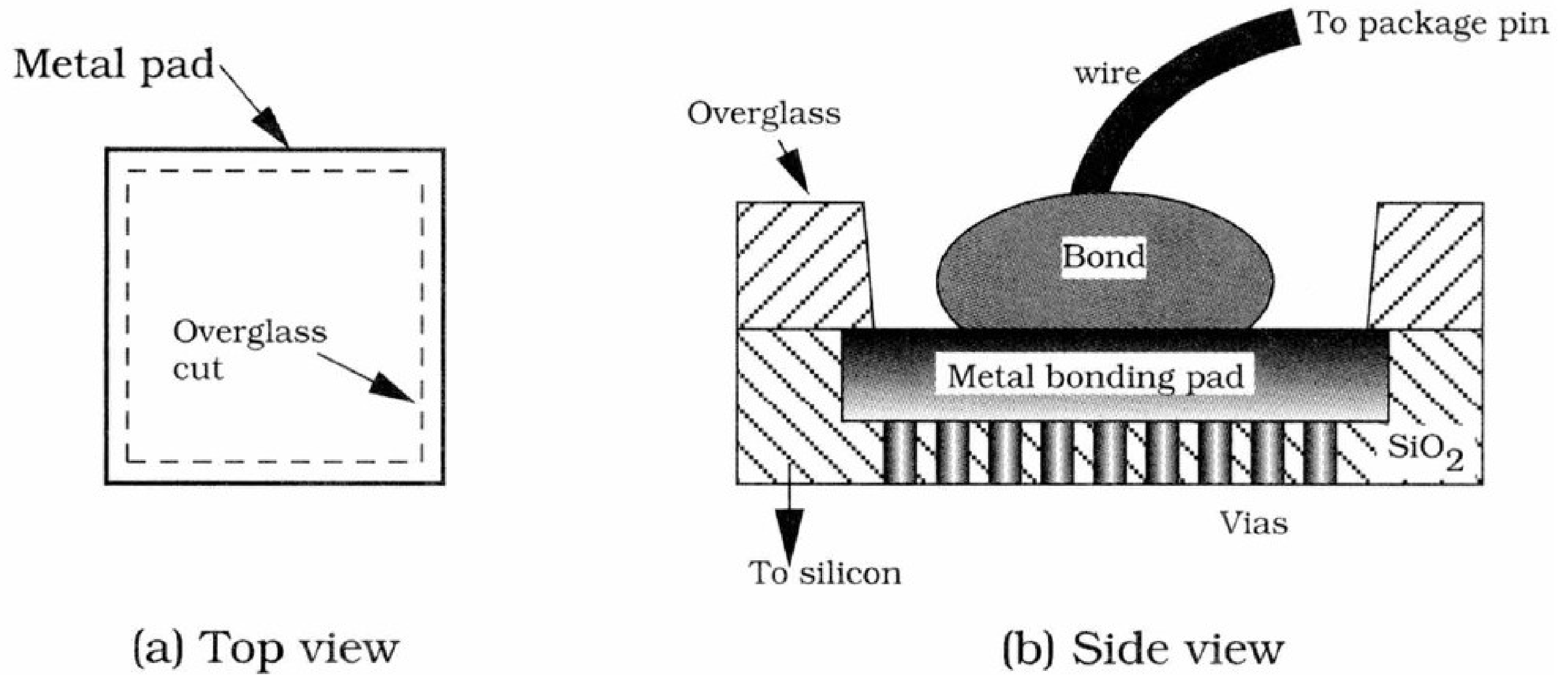


Figure 4.19 Bonding pad structure

Transistor Cross Section