ENGR354 - Digital Logic
Fall 2020

Date			Topic	Reading
M	Sept	14	Introduction, Number systems, Design process	1.1-6, notes
W		16	Terminology, Gates, Truth tables, Boolean algebra	2.1-5
F		18	Boolean Algebra, DeMorgan's laws, Synthesis	2.5-6
M		21	Synthesis, Examples	2.6-8
W		23	Logic Minimization, K-Maps	4.1-2
F		25	K-Maps, Don't Cares, Examples and practice	4.2-4
M		28	Entered variable maps	notes
W		30	Minimization using entered variable maps	notes
F	Oct	2	Logic kit, Implementation technology, data sheets	3.1-6,notes
M		5	Multiplexers	6.1
W		7	Decoders, Encoders	6.2-3
F		9	Code converters, Arithmetic circuits	6.4-5
M		12	Arithmetic circuits	5.1-5.3.2
M		14	Review and catch up	
F		16	Midterm exam 1	Chapters 1-6
M		19	Memory, the basic cell {latch}	7.1-2
W		21	Latches	7.3
F		23	Flip-Flops	7.4-7
M		26	Registers & Counters	7.8-9
W		28	Sequential Circuits - State machines, Models, State diagrams	8.1, notes
F		30	State machines	8.2-3
M	Nov	2	State machines, design examples	8.2-3
W		4	State machines, alternate methods, examples	notes
F		6	Project introduction, exam review	notes
M		9	Midterm exam 2 Emphasis on chapters 7 & 8	
W		11	Fundamental mode (asynchronous logic)	9.1
F		13	Logic hazards	9.6, notes
M		16	Language directed logic design - VHDL	6.6.1-6.6.3
W		18	More VHDL	
F		20	Wrap up	

Tuesday November 24 - Final Exam time 8 am.