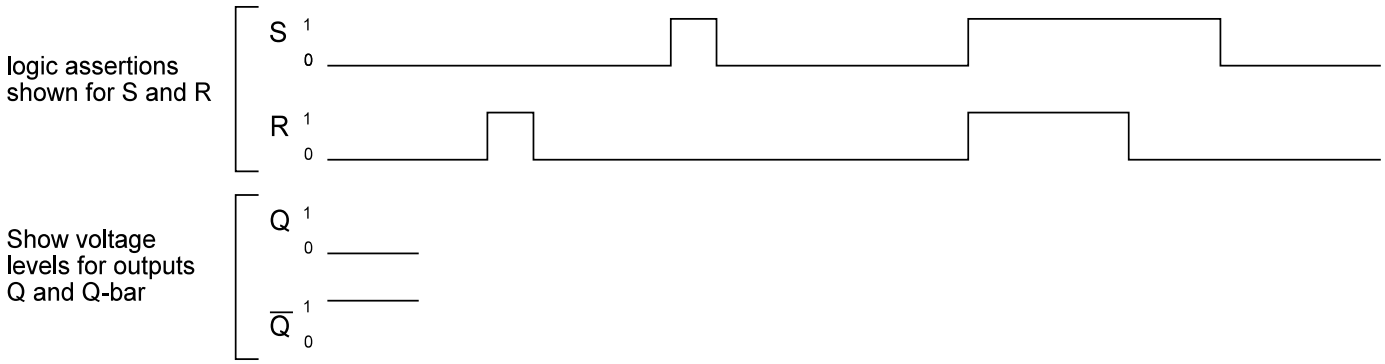
ENGR-354
HW#12

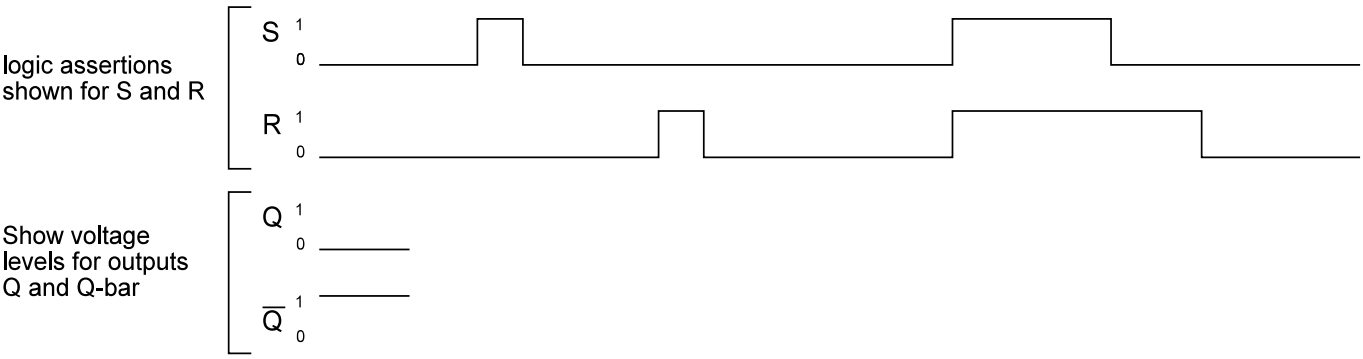
1) Below is shown a timing diagram representing the signals in and out of a Reset dominant (i.e. NOR centered) basic cell as a function of time. Complete the diagram by drawing in the Q and Q' signals.

   For the NOR centered basic cell, logic level and voltage levels of the inputs are the same, i.e. a logic one is a high voltage and logic zero a low voltage.

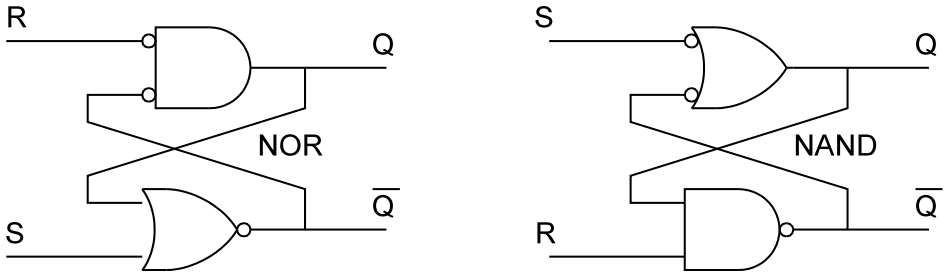


2) Below is shown a timing diagram representing the signals in and out of a Set dominant (i.e. NAND centered) basic cell as a function of time. Complete the diagram by drawing in the Q and Q' signals.

   Note that for a NAND basic cell the logic of inputs S and R is shown and that the electrical level is the opposite, i.e a logic one is a low voltage and logic zero is a high voltage. That is, when the Set input is not asserted it is at a high voltage and when it is asserted it is at a low voltage



For reference:



3) Construct the NAND centered basic cell on your bread board. Use a 74HC00 part. Refer to the pin out diagrams on the class web page. Connect switches on the I/O logic board to the S and R inputs of the basic cell. Connect the Q and Q-bar outputs to LED inputs on the I/O board. Submit a photo of your constructed circuit.

   Note that when an upper pushbutton is pressed a high voltage output occurs and pushing the mating lower button causes the output voltage to be low (about zero volts). Also, it takes a high voltage on the LED inputs to light up an LED.