Comments on HW#12 problem 2

Problem 2 is about the NAND centered basic cell. Below are three ways to draw the circuit, all using NAND gates but in figures 2 and 3 the DeMorgan theorem is applied. Figure 1 shows the basic cell drawn with the NAND gate symbol. Figure 2 more clearly shows that if a low voltage is applied to the set terminal it will cause the Q output to go to a high voltage. Figure 3 more clearly shows the same for the reset input.

In summary, for the set and reset signals to not be asserted, i.e. false, they need to be at a high voltage. When at a low voltage, the set or reset signals are asserted which means true. A challenge then is to understand what we mean by a 0 or a 1. And it should be noted that not all authors or bloggers use it consistently or in the same way.

Fig. 1

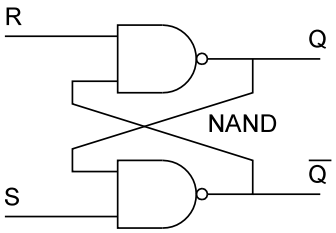


Fig. 2

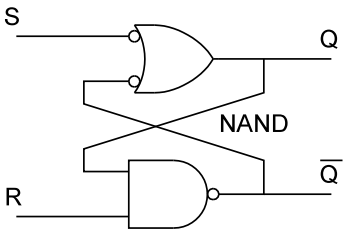
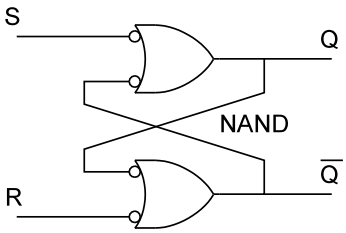


Fig. 3



You likely have heard me use the term “asserted” which I equate with logic true and the term “not asserted” logic false. The term asserted doesn’t define whether the voltage is high or low, just true or false. The phrase “asserted high” implies that a high voltage represents true while “asserted low”implies that a low voltage represents true. Some authors will state “active high” or “active low” in the same way.

So, when creating a truth table or similar how should 1's and 0's be used? I recommend that normally ‘1' represent true and ‘0' represent false and not high voltage or low voltage. In the slides shown in class the excitation tables for NAND and NOR basic cells were shown this way:

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	ϕ
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	1	ϕ
	ϕ	0

Excitation Table NAND-centered

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
	ϕ	1
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	ϕ	1
$1 \rightarrow 1$	ϕ	0

Excitation Table NOR-centered

Note that for the 0- to-1 transition in both tables that S is a ‘1' even though for the NAND cell S has to be at a low voltage for set to occur and at a high voltage for the NOR cell. In these tables a ‘1' represents true, not high voltage.

Thus in problem 2 the timing diagram shows S and R as logic ‘1' when they are true even though the voltage at that point would be low. Note that for the Q and Q-bar outputs that you are asked to draw, a high voltage will indicate logic ‘1' on the Q output while at the same time the Q-bar output will be at a low voltage.