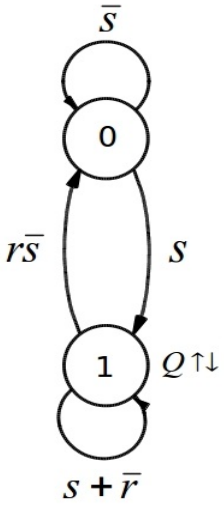
ENGR-354
HW # 13

1) A Set-Reset flip-flop has set and reset inputs like a gated SR latch. Design a rising edge Set-Reset flip-flop using a rising edge D flip-flop and other logic gates. Draw the circuit.

   Note that clock connects only to the clock input of the D flip-flop. We say that the flip-flop that is being designed inherits clock behavior (i.e. rising or fall edge triggering) from the D flip-flop.

   The state diagram and SR operation table show how the assertion of S and R affect the output Q (the state diagram is a graphical way to show the operation table). The D-F/F excitation table defines how the D input needs to be asserted to make transitions state to state.



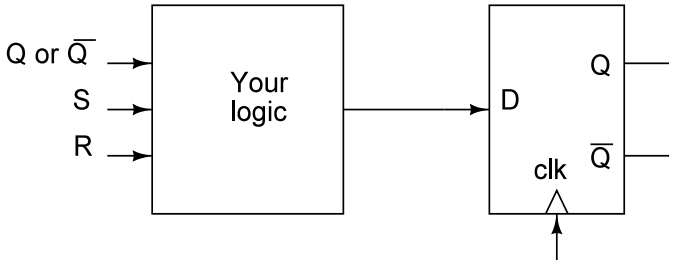
State Diagram

S	R	Action	Q_{N+1}
0	0	hold	Q_N
0	1	reset	0
1	0	set	1
1	1	set	1

Operation Table

$Q_n \rightarrow Q_{n+1}$	D
$0 \rightarrow 0$	0
$0 \rightarrow 1$	1
$1 \rightarrow 0$	0
$1 \rightarrow 1$	1

D-F/F excitation table



Block diagram of the SR flip flop you are designing.

2) Repeat problem one but use the operation table shown below. Draw the circuit. Also draw the state diagram.

S	R	Action	Q_{n+1}
0	0	hold	Q_n
0	1	reset	0
1	0	set	1
1	1	reset	0

Operation Table