Sequential Logic Elements

Latches

Circuit Types

- ***Combinational*** – output depends only on the input.
- ***Sequential*** – output depends on input and past behavior
  - Requires use of storage elements;
  - Contents of the storage elements is called *state;*
  - Circuit goes through a sequence of states as a result of changes in inputs.
- ***Synchronous*** – controlled by a clock.

Clock Signals

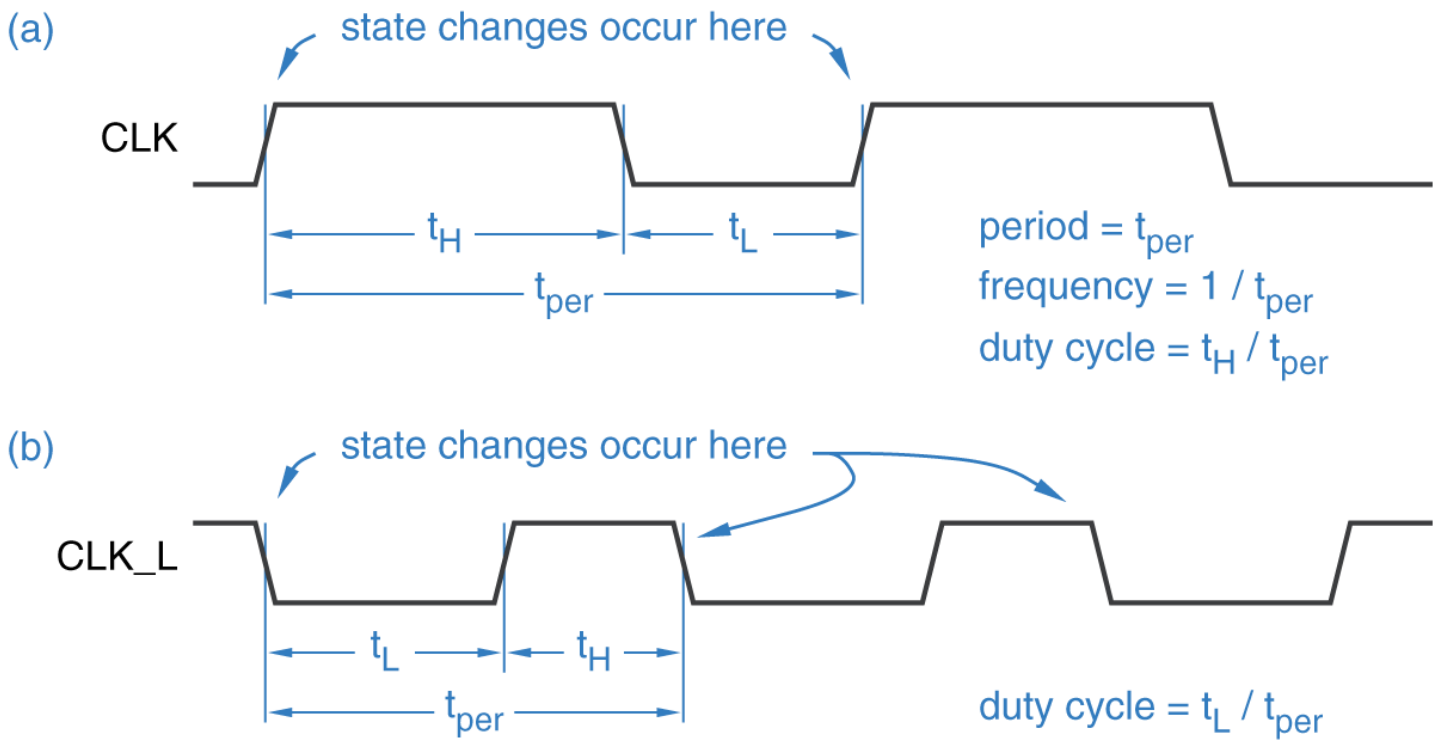
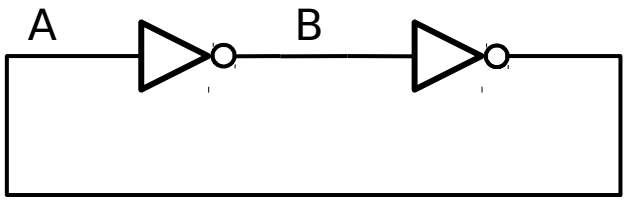


Figure 7-1

Clock signals: (a) active high; (b) active low.

A Bistable Memory Element

- Bistable – possessing two stable states.



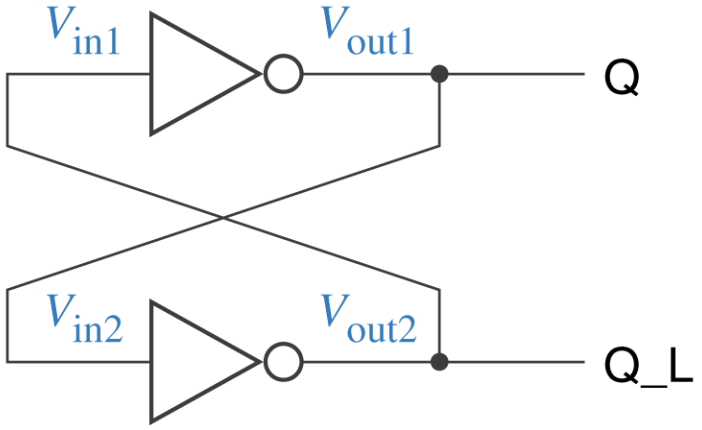


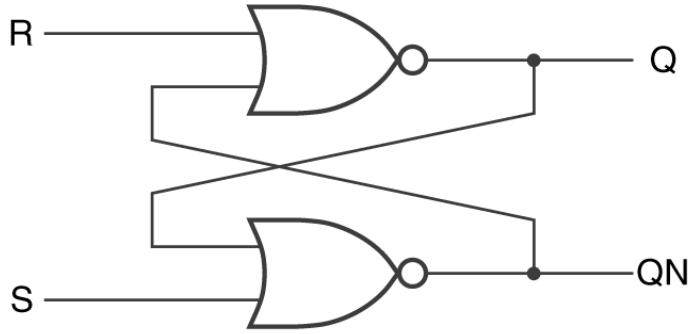
Figure 7-2

A pair of inverters forming a bistable element.

A Set/Reset (SR) Memory Element

- Called a ***Basic Cell;***
- NOR centered Basic Cell:
  - Circuit (a), Function table (b).
- Inputs are active when they are ***high;***
- Blocking side inputs.

(a)

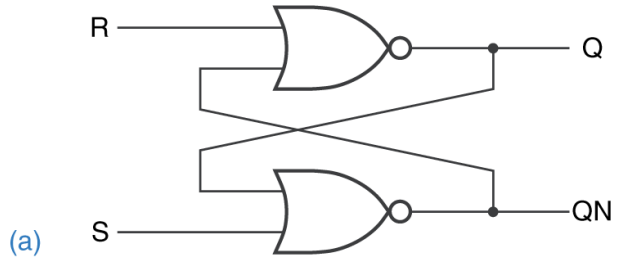


(b)

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

Typical Operation of a *Basic Cell*

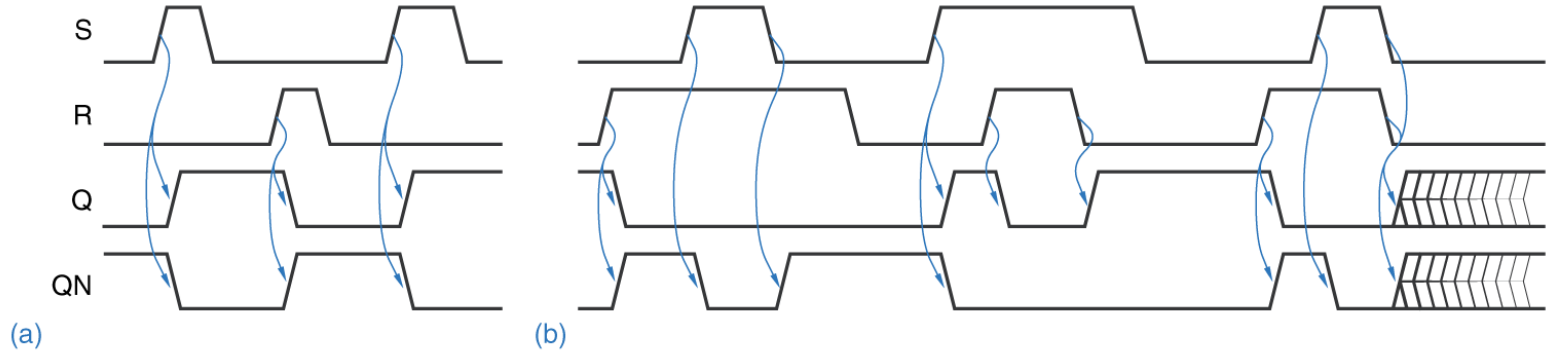
- Reset, clear.
- Set, preset.



(a)

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

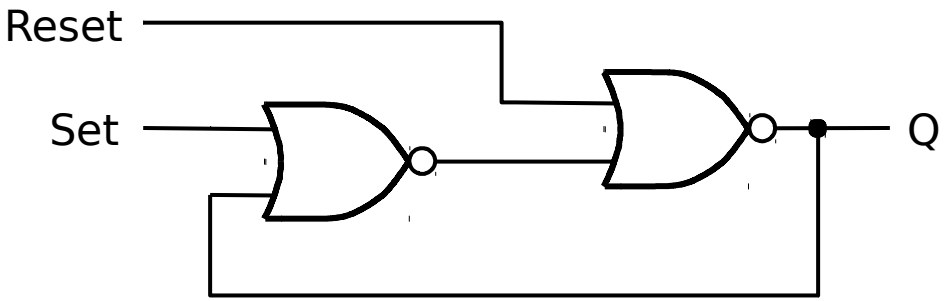
(b)



(a) (b)

(a) (b)

NOR-Centered (Reset Dominant) Basic Cell



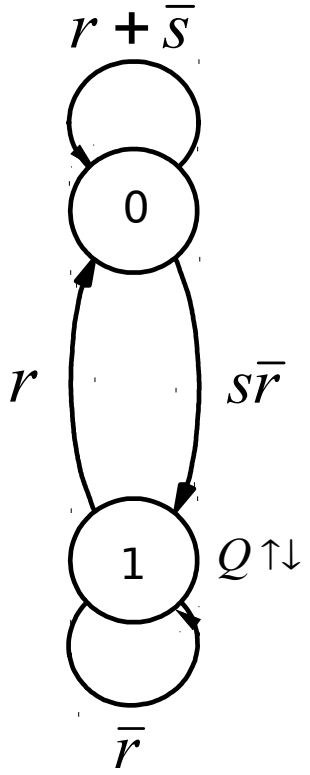
Circuit

S	R	Action	Q_{n+1}
0	0	hold	Q_n
0	1	reset	0
1	0	set	1
1	1	reset	0

Operation Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
	ϕ	1
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	ϕ	1
$1 \rightarrow 1$	ϕ	0

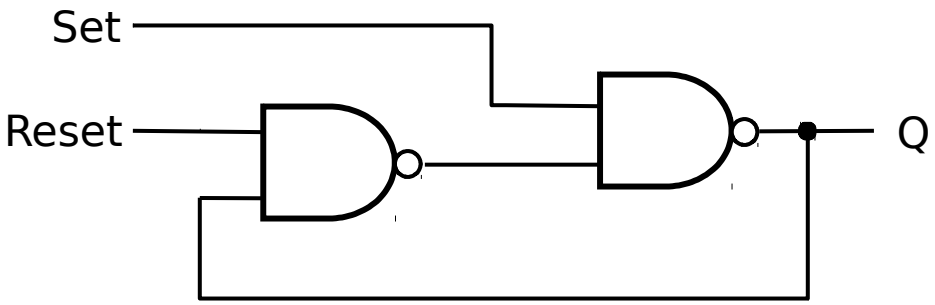
Excitation Table



State Diagram

NAND-Centered (Set Dominant) Basic Cell

- Inputs are active low (when they are ***asserted***);
- Operation table indicates assertion, not voltage, levels.



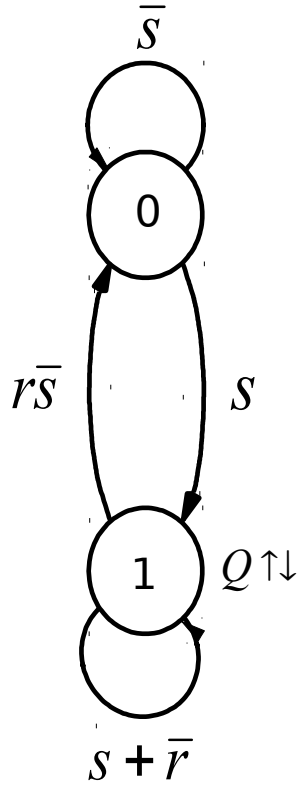
Circuit

S	R	Action	Q_{N+1}
0	0	hold	Q_N
0	1	reset	0
1	0	set	1
1	1	set	1

Operation Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	ϕ
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	1	ϕ
	ϕ	0

Excitation Table



State Diagram

Combined Form of the Basic Cell

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	ϕ
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	1	ϕ
	ϕ	0

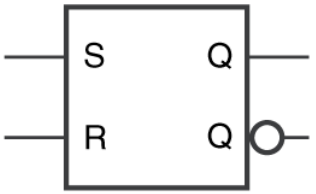
Excitation Table NAND-centered

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
	ϕ	1
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	ϕ	1
$1 \rightarrow 1$	ϕ	0

Excitation Table NOR-centered

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

Excitation Table Combined Form



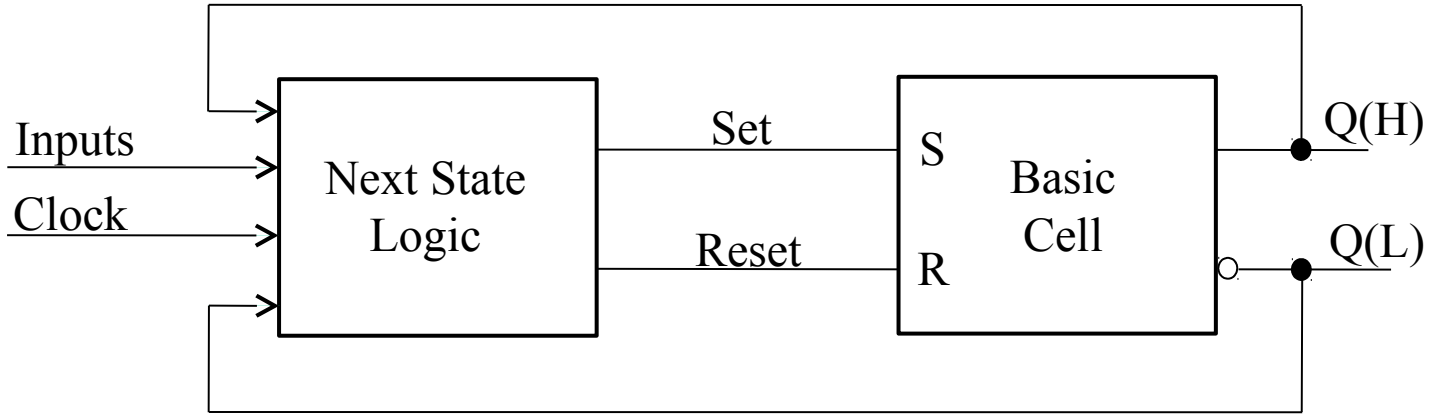
Basic Cell

Designing Latches - A Model

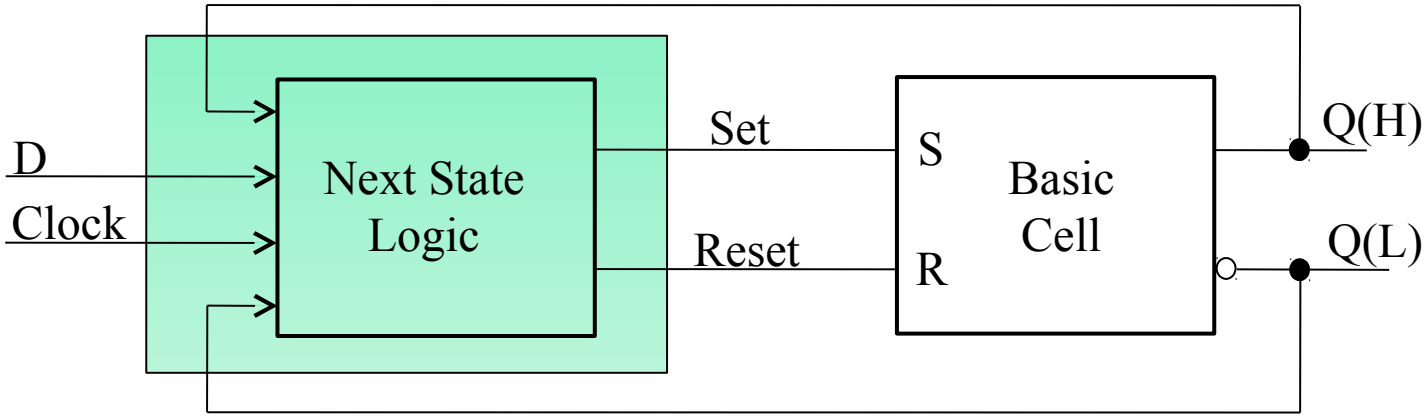
- Latch - a logic circuit that transfers the input state to the output state when the *clock* signal is high and latches and holds the input when the *clock* signal goes low.

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

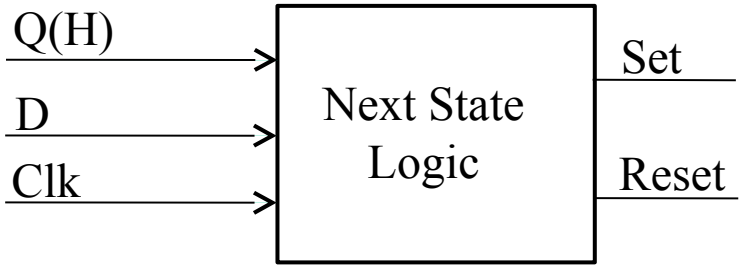
Excitation Table Combined Form



Design of a Clocked D (Data) Latch



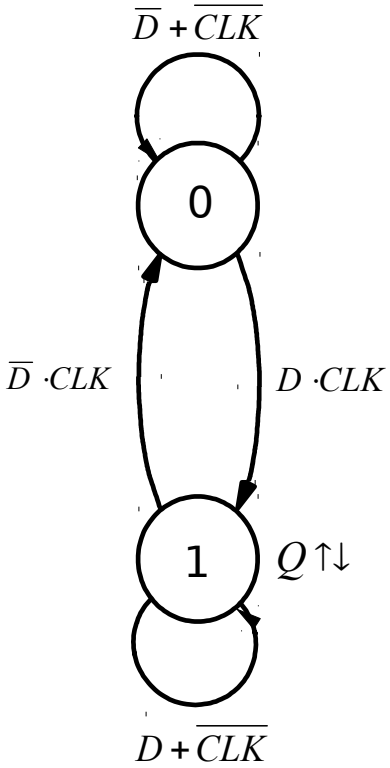
Design of a Clocked D Latch



Block Diagram

Clk	D	Qn	Qn+1	Set	Reset
0	0	0	0	0	ϕ
0	0	1	1	ϕ	0
0	1	0	0	0	ϕ
0	1	1	1	ϕ	0
1	0	0	0	0	ϕ
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	1	ϕ	0

Truth Table



State Diagram

Clk	D	Action	Q_{N+1}
0	x	hold	Q_N
1	0	reset	0
1	1	set	1

Operation Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

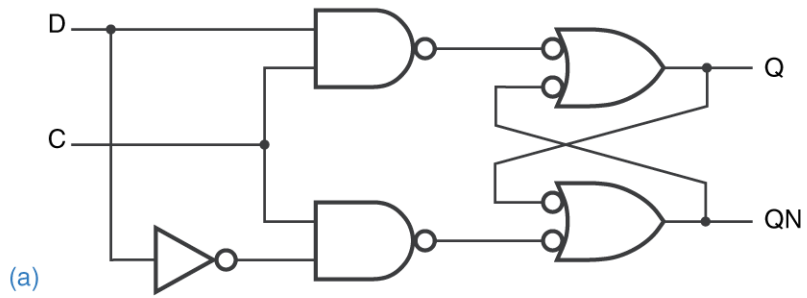
Excitation Table Basic Cell

$$Set = clk \cdot D$$

$$Reset = clk \cdot \overline{D}$$

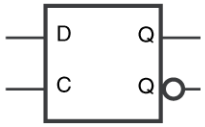
Equations

Clocked D Latch



C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

(b)



(c)

Figure 7-12

D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

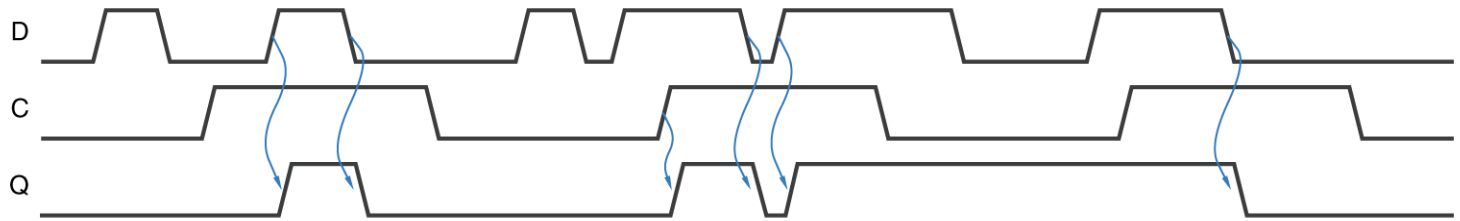
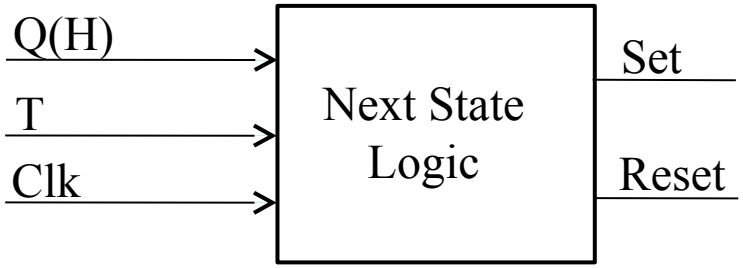


Figure 7-13

Functional behavior of a D latch for various inputs.

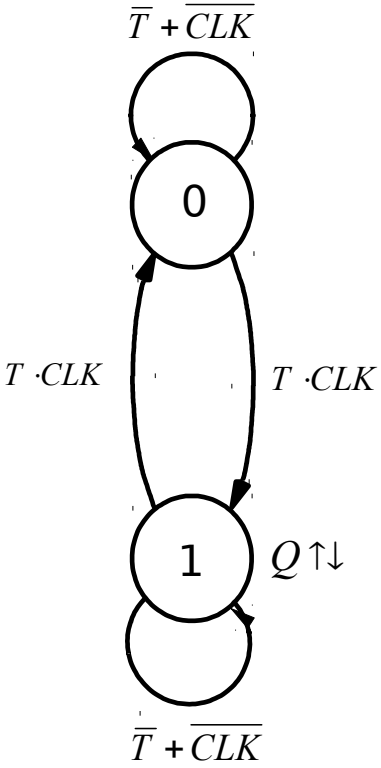
Design of a Clocked Toggle (T) Latch



Block Diagram

Clk	T	Qn	Qn+1	Set	Reset
0	0	0	0	0	ϕ
0	0	1	1	ϕ	0
0	1	0	0	0	ϕ
0	1	1	1	ϕ	0
1	0	0	0	0	ϕ
1	0	1	1	ϕ	0
1	1	0	1	1	0
1	1	1	0	0	1

Truth Table



State Diagram

Clk	T	Action	Q_{N+1}
0	x	Hold	Q_N
1	0	Hold	Q_N
1	1	Toggle	$\overline{Q}_N$

Function Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

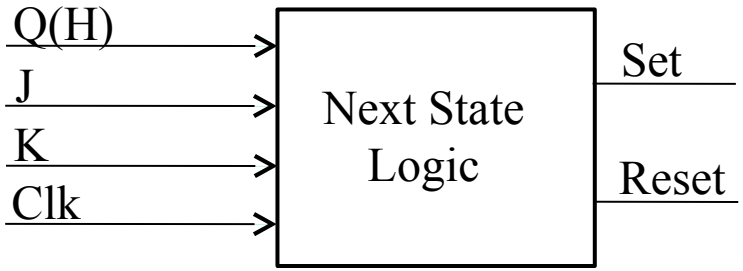
Excitation Table Basic Cell

$$Set = clk \cdot T \cdot \overline{Q}$$

$$Reset = clk \cdot T \cdot Q$$

Equations

Design of a Clocked JK Latch



Block Diagram

Clk	J	K	Qn	Qn+1	Set	Reset
0	0	0	0	0	0	ϕ
0	0	0	1	1	ϕ	0
0	0	1	0	0	0	ϕ
0	0	1	1	1	ϕ	0
0	1	0	0	0	0	ϕ
0	1	0	1	1	ϕ	0
0	1	1	0	0	0	ϕ
0	1	1	1	1	ϕ	0
1	0	0	0	0	0	ϕ
1	0	0	1	1	ϕ	0
1	0	1	0	0	0	ϕ
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	0	1	1	ϕ	0
1	1	1	0	1	1	0
1	1	1	1	0	0	1

Truth Table

Clk	J	K	Action	Q_{N+1}
0	x	x	Hold	Q_N
1	0	0	Hold	Q_N
1	0	1	Reset	0
1	1	0	Set	1
1	1	1	Toggle	$\overline{Q}_N$

Function Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

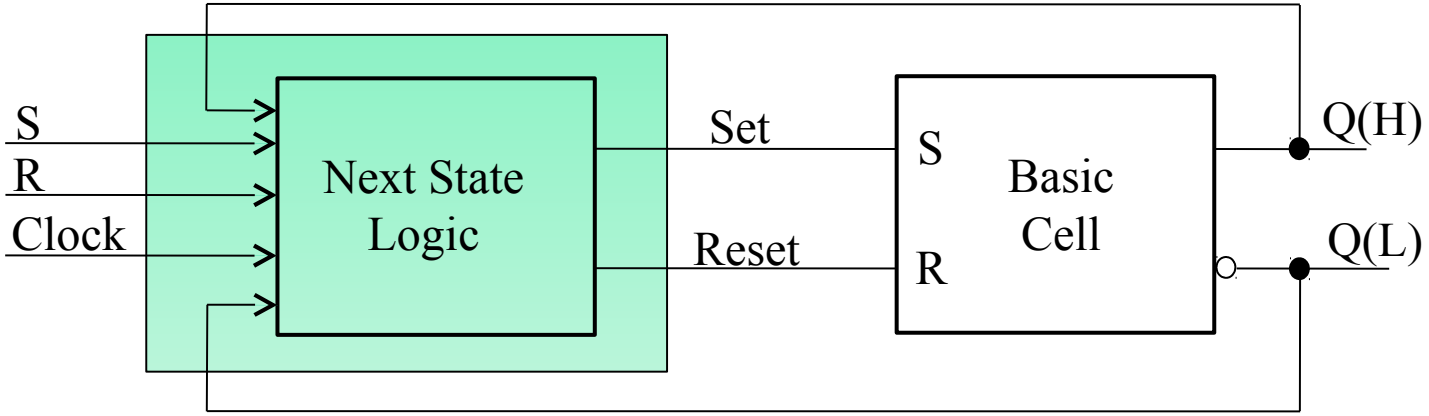
Excitation Table
Basic Cell

$$Set = clk \cdot J \cdot \overline{Q}$$

$$Reset = clk \cdot K \cdot Q$$

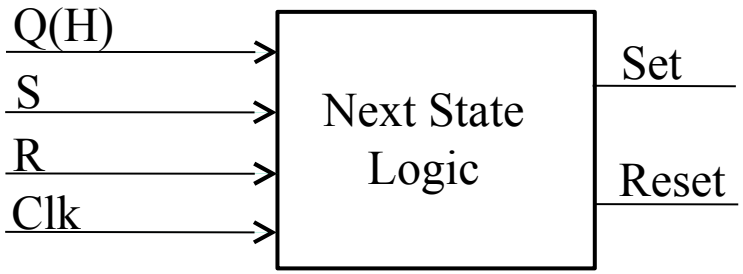
Equations

Design of a Set-Dominant Clocked SR Latch



- Inputs – S, R, Clock, Q
- Outputs – Set, Reset

Design of a Set-Dominant Clocked SR Latch



Block Diagram

S	R	Action	Q_{N+1}
0	0	hold	Q_N
0	1	reset	0
1	0	set	1
1	1	set	1

Operation Table

$Q_n \rightarrow Q_{n+1}$	Inputs S	R
$0 \rightarrow 0$	0	ϕ
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	ϕ	0

Excitation Table Basic Cell

$$Set = clk \cdot S$$

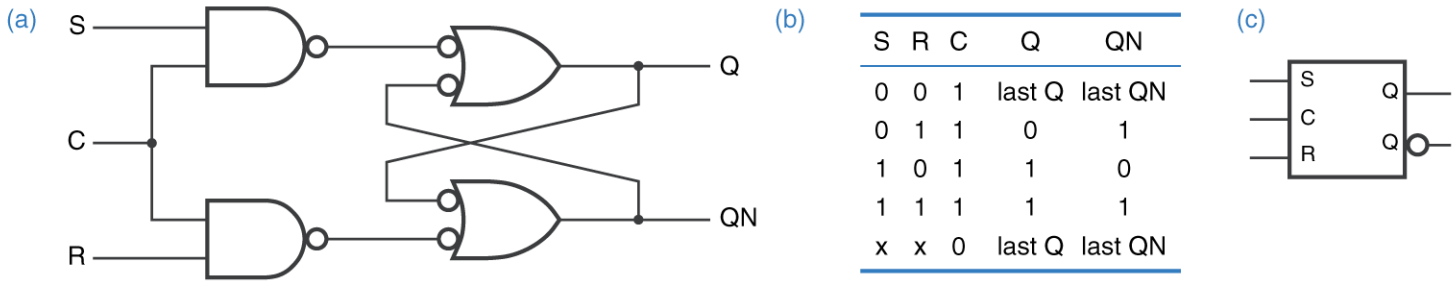
$$Reset = clk \cdot R \cdot \overline{S}$$

Equations

Clk	S	R	Qn	Qn+1	Set	Reset
0	0	0	0	0	0	ϕ
0	0	0	1	1	ϕ	0
0	0	1	0	0	0	ϕ
0	0	1	1	1	ϕ	0
0	1	0	0	0	0	ϕ
0	1	0	1	1	ϕ	0
0	1	1	0	0	0	ϕ
0	1	1	1	1	ϕ	0
1	0	0	0	0	0	ϕ
1	0	0	1	1	ϕ	0
1	0	1	0	0	0	ϕ
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	0	1	1	ϕ	0
1	1	1	0	1	1	0
1	1	1	1	1	ϕ	0

Truth Table

SR Latch with Enable (Clock)



S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

Figure 7-10

S-R latch with enable: (a) circuit using NAND gates; (b) function table; (c) logic symbol.

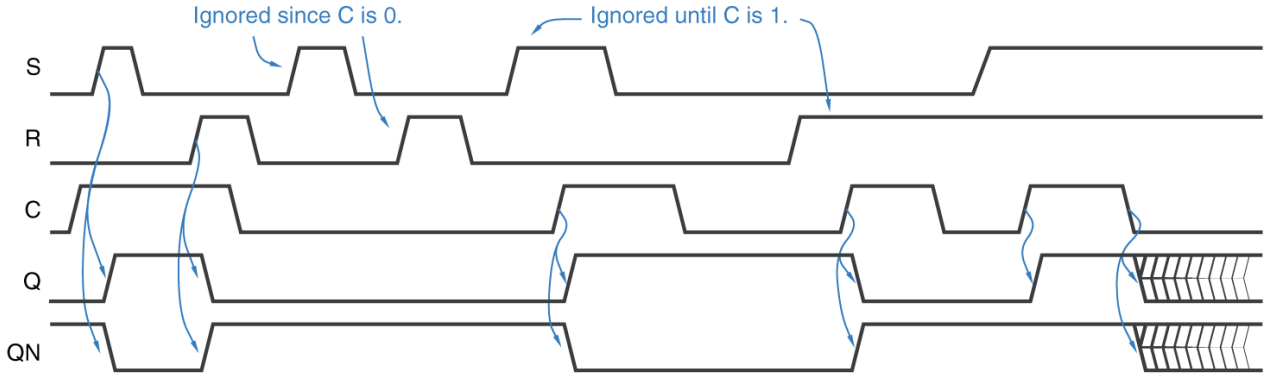
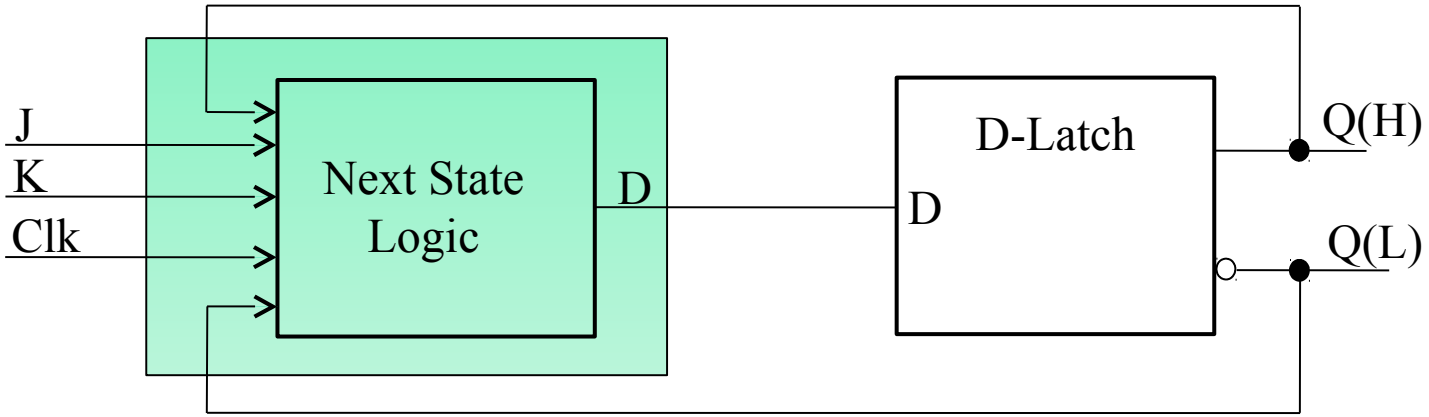


Figure 7-11

Typical operation of an S-R latch with enable.

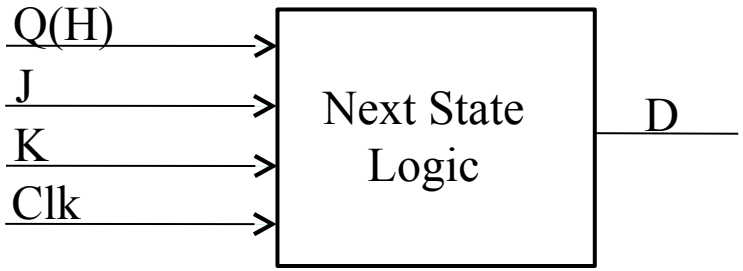
Design of a Clocked JK Latch – Version II

- Replace the basic cell with a D-latch as the memory element.



- Inputs – J, K, Clk, Q
- Output – D

Design of a Clocked JK Latch – Version II



Block Diagram

Clk	J	K	Qn	Qn+1	D
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	0

Truth Table

Clk	J	K	Action	Q_{N+1}
0	x	x	Hold	Q_N
1	0	0	Hold	Q_N
1	0	1	Reset	0
1	1	0	Set	1
1	1	1	Toggle	$\overline{Q}_N$

Function Table

$Q_n \rightarrow Q_{n+1}$	D
$0 \rightarrow 0$	0
$0 \rightarrow 1$	1
$1 \rightarrow 0$	0
$1 \rightarrow 1$	1

Excitation Table

$$D = \overline{K} \cdot Q + Q \cdot \overline{clk} + clk \cdot J \cdot \overline{Q}$$

Equation

Terminology

- Latches are often called ***Transparent*** because the output will follow the input as long as the clock signal is high.
- Flip-flops are ***edge-triggered***
  - Positive-edge triggered (PET) is when action occurs on the rising edge of the clock signal;
  - Negative-edge triggered (NET) is when action occurs on the falling edge of the clock signal.
- Types of Flip-flops
  - SR (rarely used);
  - D (very, very common, 74HC74);
  - JK (hardly ever used, 74HC109);
  - Toggle (occasionally used by CAD programs).