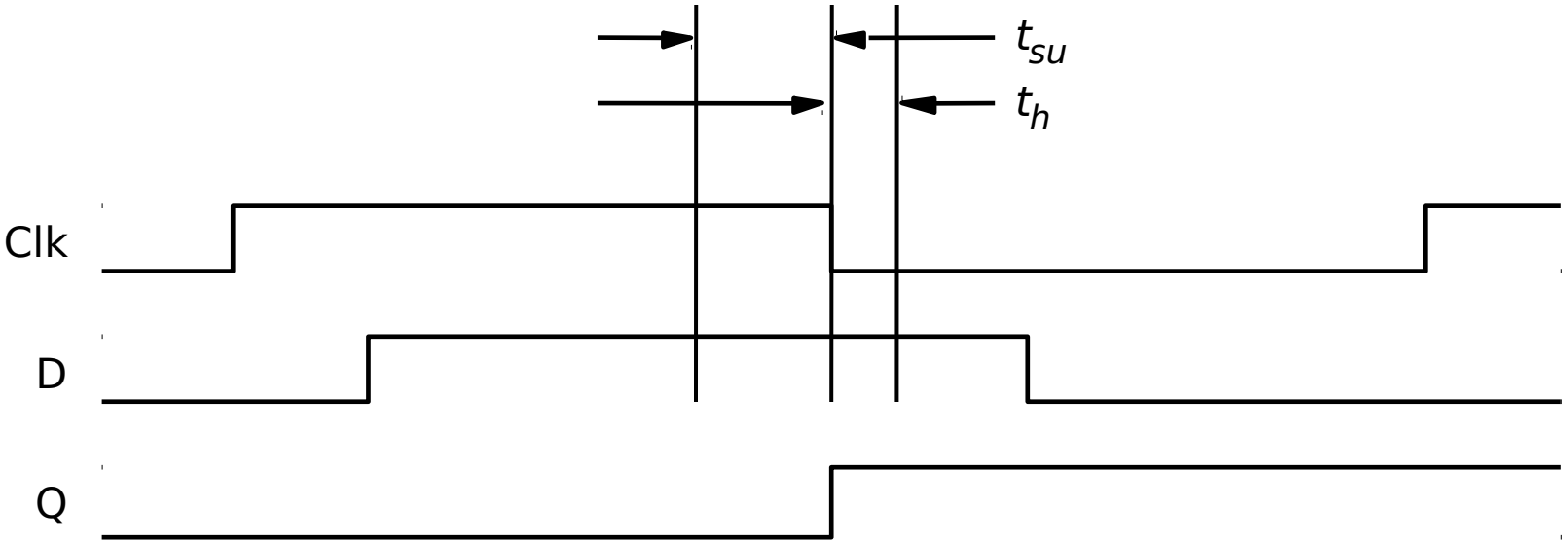
Flip-Flops

Terminology

- Latches are often called ***Transparent*** because the output will follow the input as long as the clock signal is high.
- Flip-flops are ***edge-triggered***
  - Positive-edge triggered (PET) is when action occurs on the rising edge of the clock signal;
  - Negative-edge triggered (NET) is when action occurs on the falling edge of the clock signal.
- Types of Flip-flops
  - SR (rarely used);
  - D (very, very common, 74HC74);
  - JK (hardly ever used, 74HC109);
  - Toggle (occasionally used by CAD programs).

Setup and Hold Times

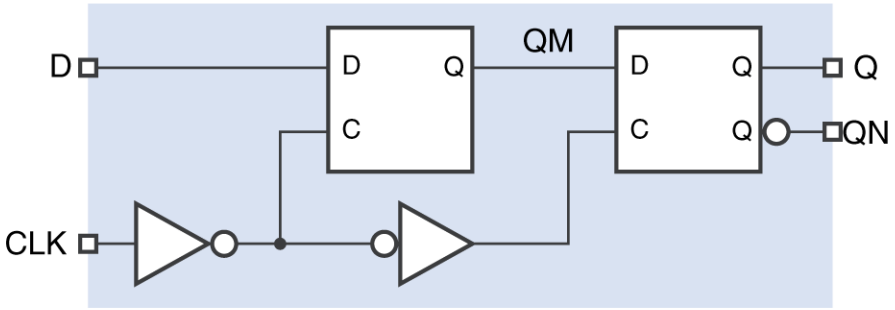
- Setup time (t_{SU}) is the time interval preceding the active transition point of the CLK during which all data inputs must remain stable.
- Hold time (t_H) is the time interval following the active transition point of the CLK during which all data inputs must remain stable.
- See data sheet for 74HC74



PET Master-Slave D Flip-Flop (Positive Edge Triggered)

- QM follows the D input whenever CLK is low.
- When CLK goes high, QM is transferred to the output.

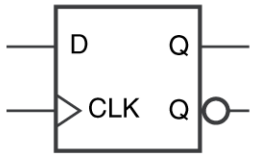
(a)



(b)

D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

(c)



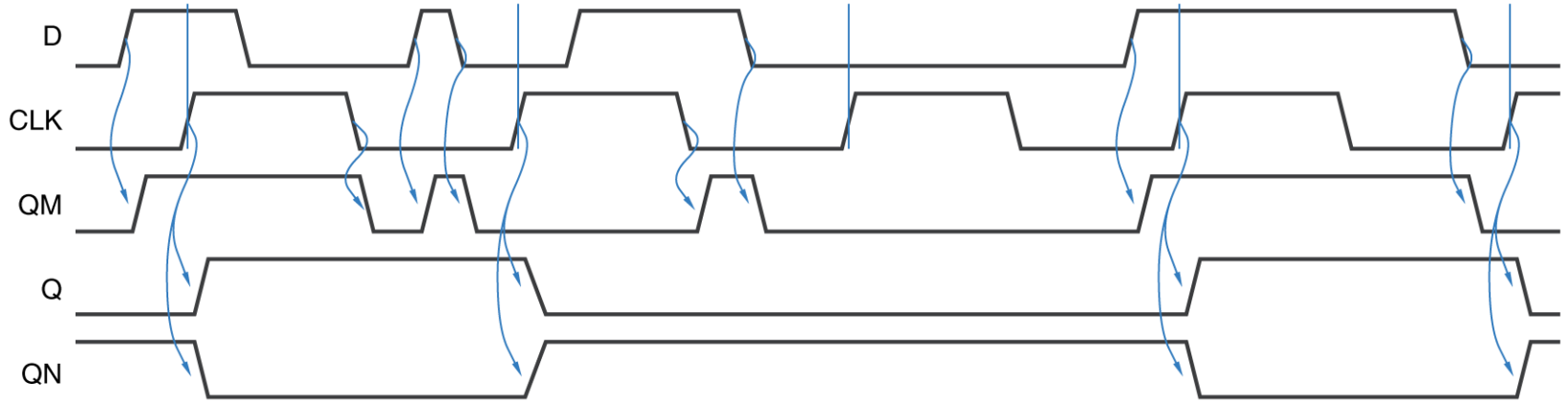


Figure 7-16

Functional behavior of a positive-edge-triggered D flip-flop.

Positive-Edge-Triggered D Flip-Flop

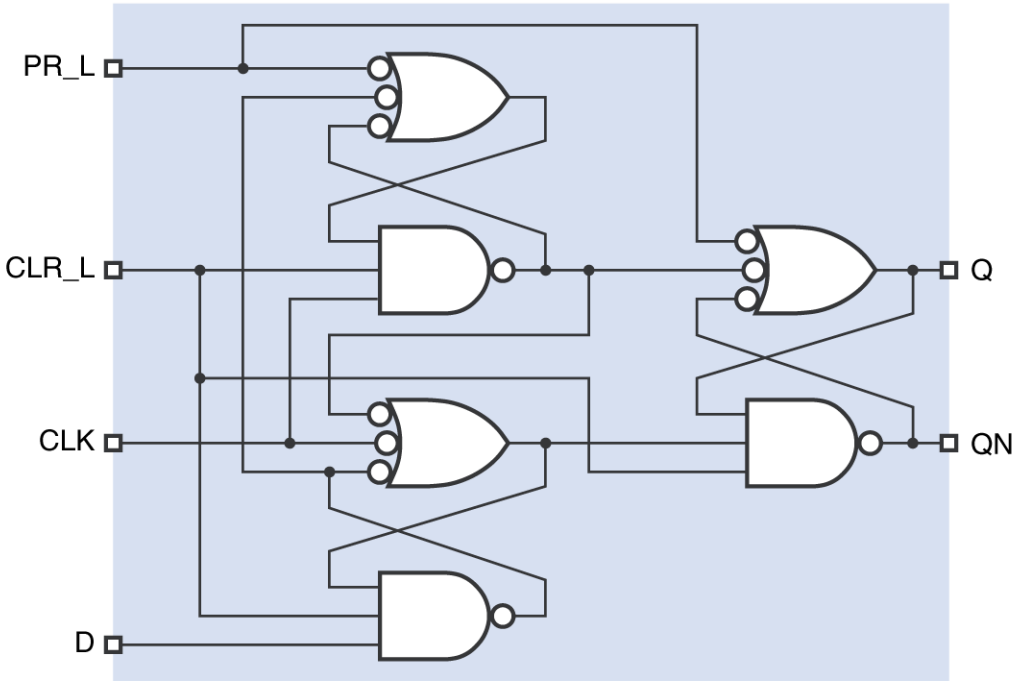


Figure 7-20

Commercial circuit for a positive-edge-triggered D flip-flop such as 74LS74.

PET D Flip-Flop with *Clear* and *Preset*

- Synchronous – transitions or actions occur in relation to the CLK signal;
- Asynchronous – transitions or actions are not related to the CLK signal.

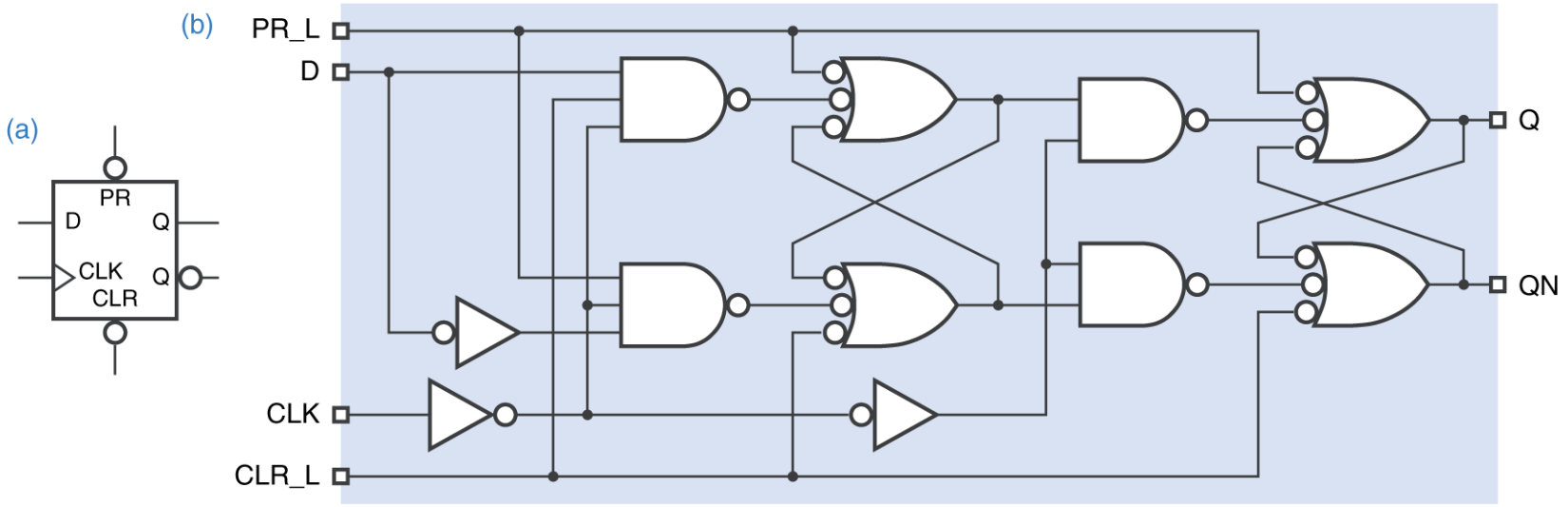
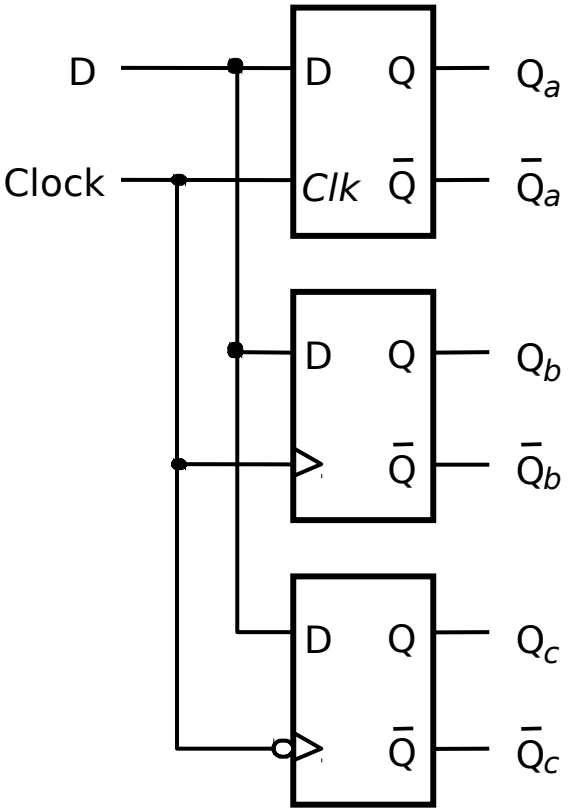


Figure 7-19

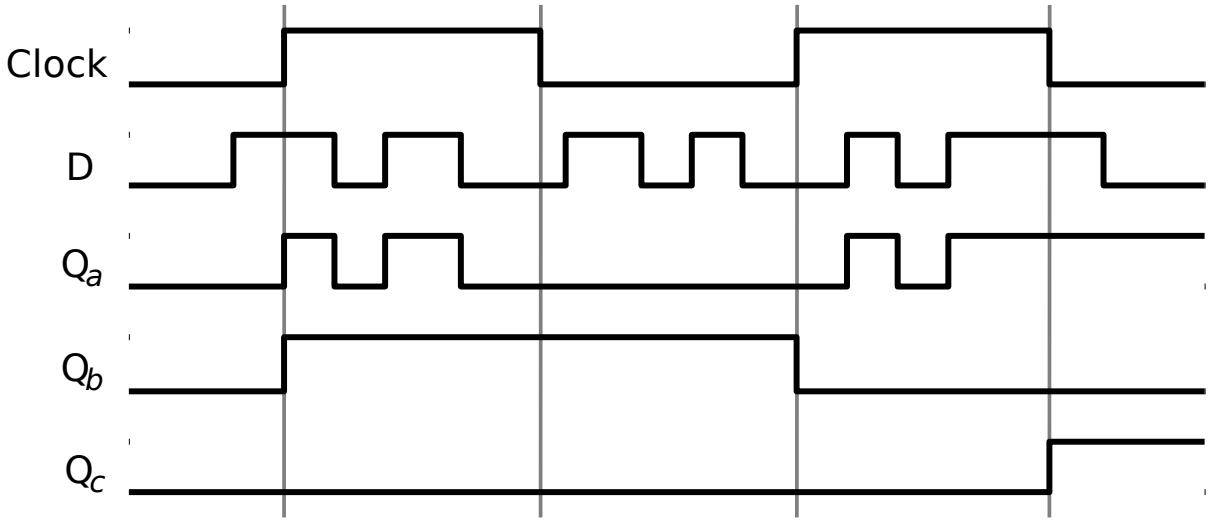
Positive-edge-triggered D flip-flop with preset and clear: (a) logic symbol; (b) circuit design using NAND gates.

Level-Sensitive vs. Edge-Triggered

- Level-sensitive = latch
- Edge-triggered = flip-flop



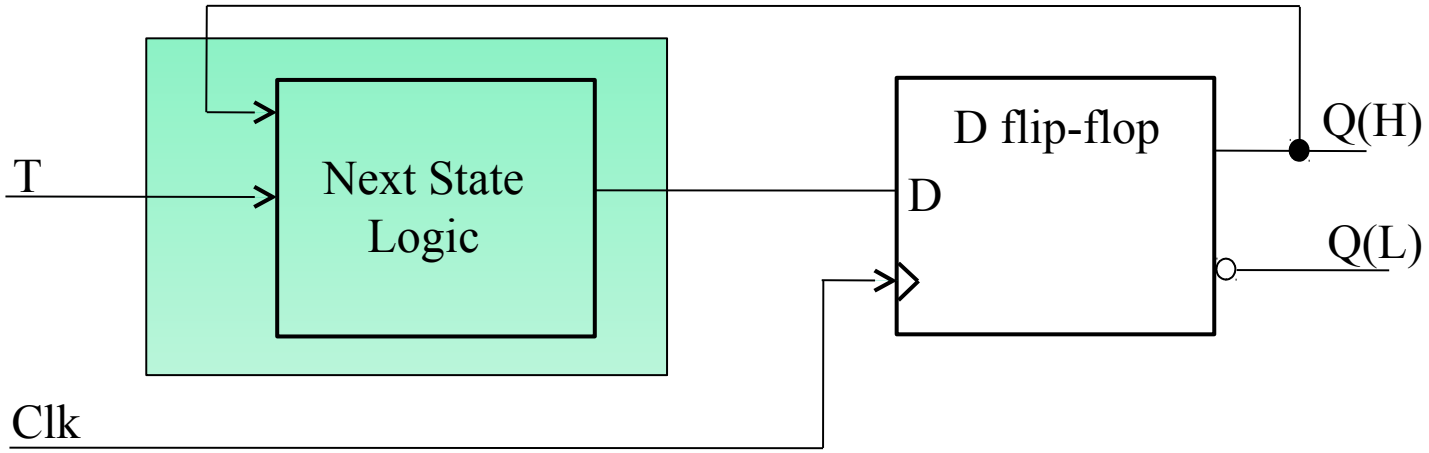
(a) Circuit



(b) Timing diagram

Design a T Flip-Flop from a D Flip-Flop

- The memory element is now ***edge-triggered*** meaning the Clk signal is no longer part of the ***next-state logic***.



T	Q(n+1)
0	Q(*n*)
1	$\bar{Q}$(*n*)

Function Table

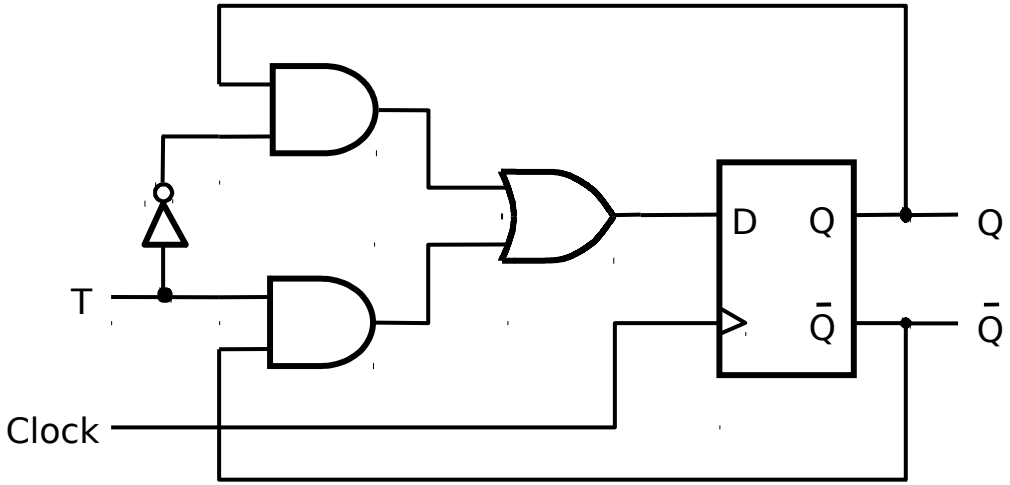
$Q_n \rightarrow Q_{n+1}$	D
$0 \rightarrow 0$	0
$0 \rightarrow 1$	1
$1 \rightarrow 0$	0
$1 \rightarrow 1$	1

Excitation Table

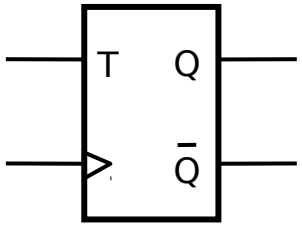
T	Qn	Qn+1	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Truth Table

Design a T Flip-Flop from a D Flip-Flop

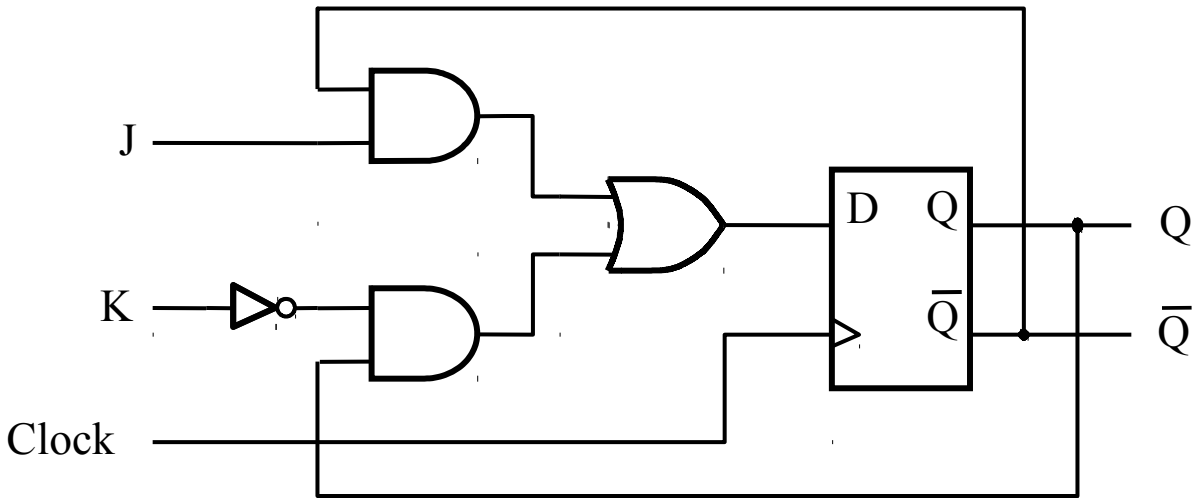


(a) Circuit



(c) Graphical symbol

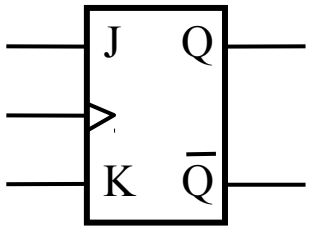
Design a JK Flip-Flop from a D Flip-Flop



Circuit

J	K	Q (n+1)
0	0	Q (n)
0	1	0
1	0	1
1	1	$\overline{Q}$ (n)

Function Table



Graphical symbol

Summary of Terminology

- Basic cell – cross-coupled NAND/NOR.
- Gated latch – output changes only while *Clk* is asserted
  - Gated SR latch;
  - Gated D latch;
  - Gated JK latch.
- Flip-flop – output changes only on *Clk* edge
  - Master-slave;
  - Edge-triggered;
  - Three main types
    - D (very, very common, 74HC74);
    - JK (hardly ever used, 74HC109);
    - Toggle (occasionally used by CAD programs).