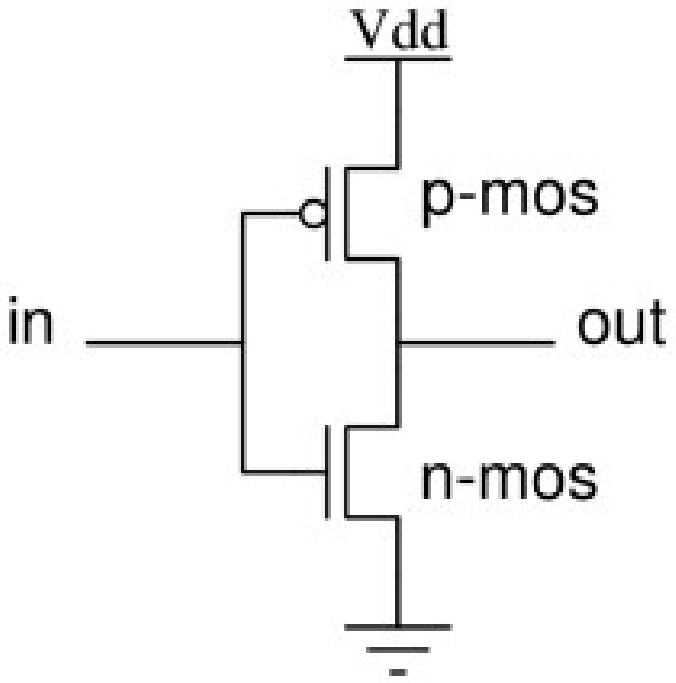
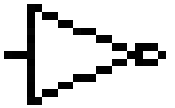
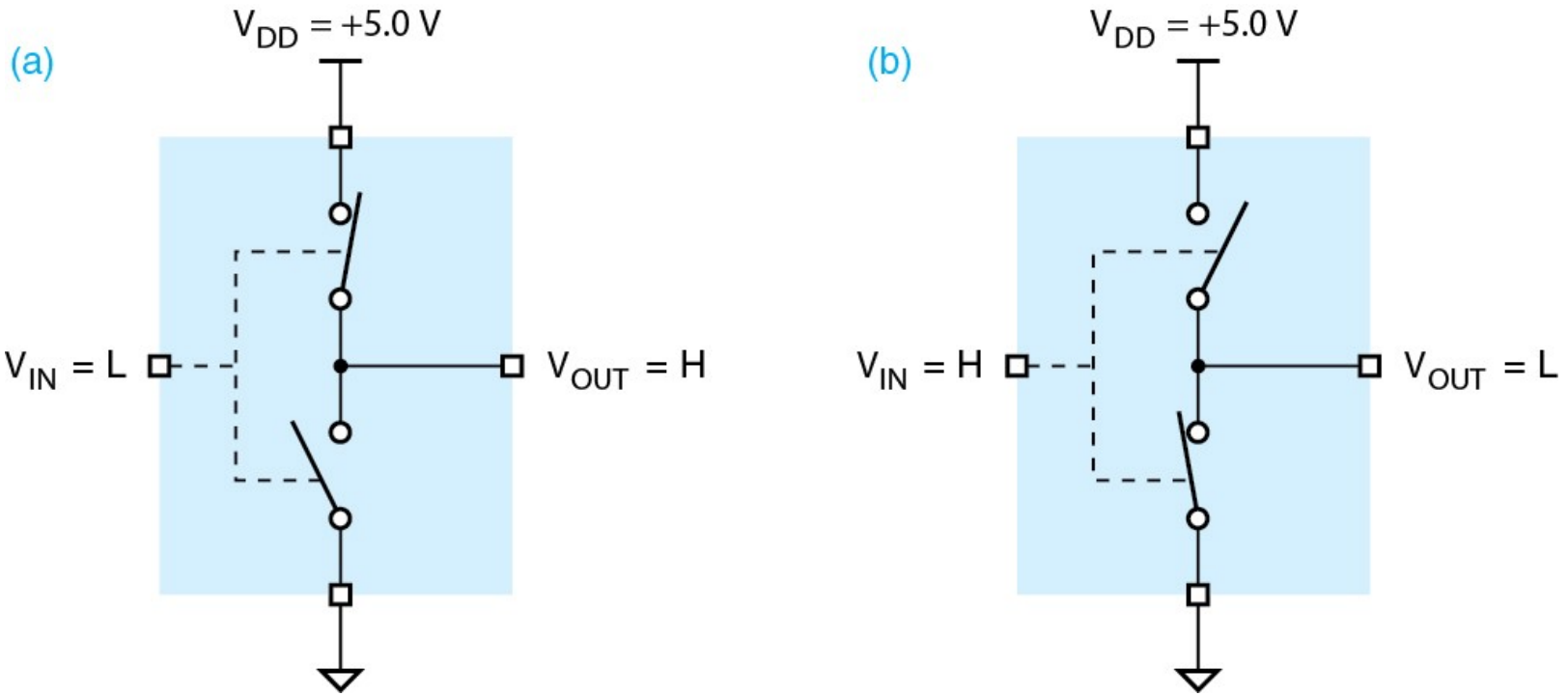
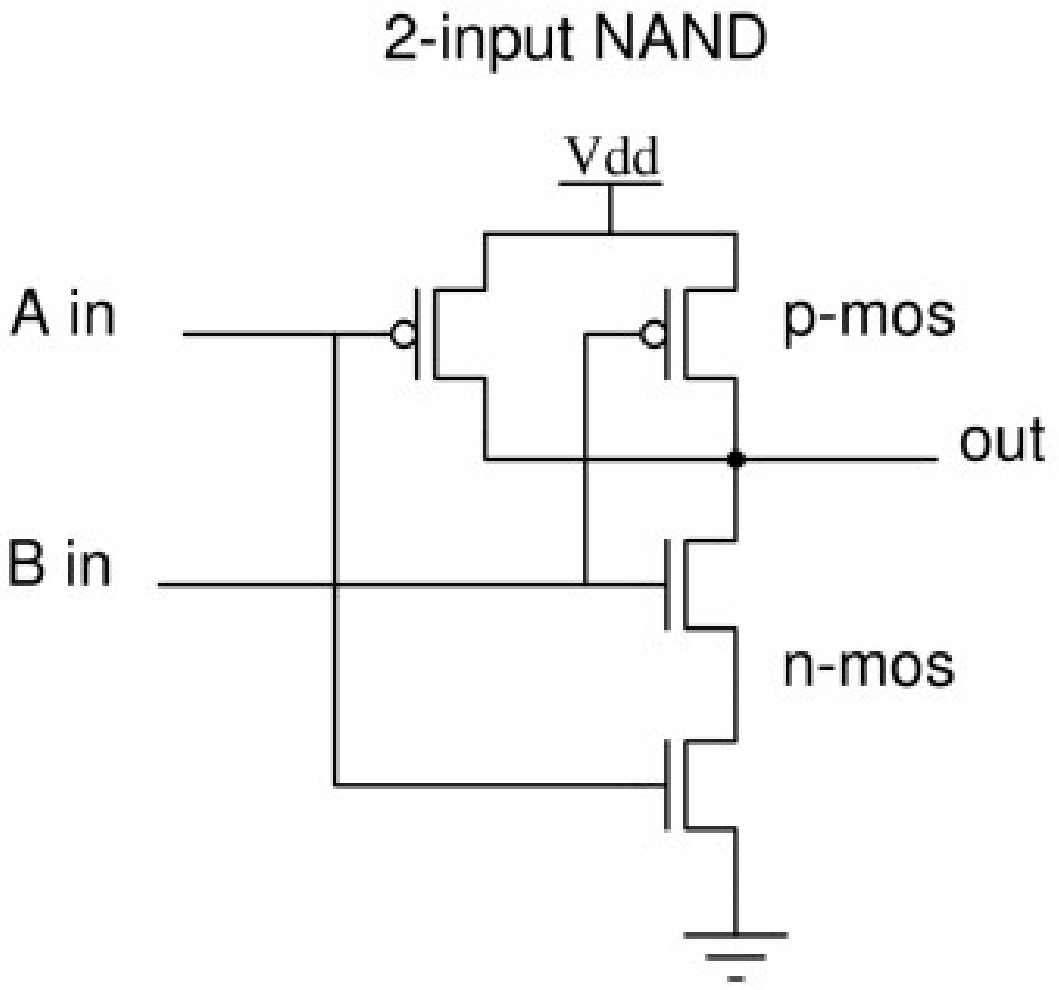
The Electronics of Logic Circuits

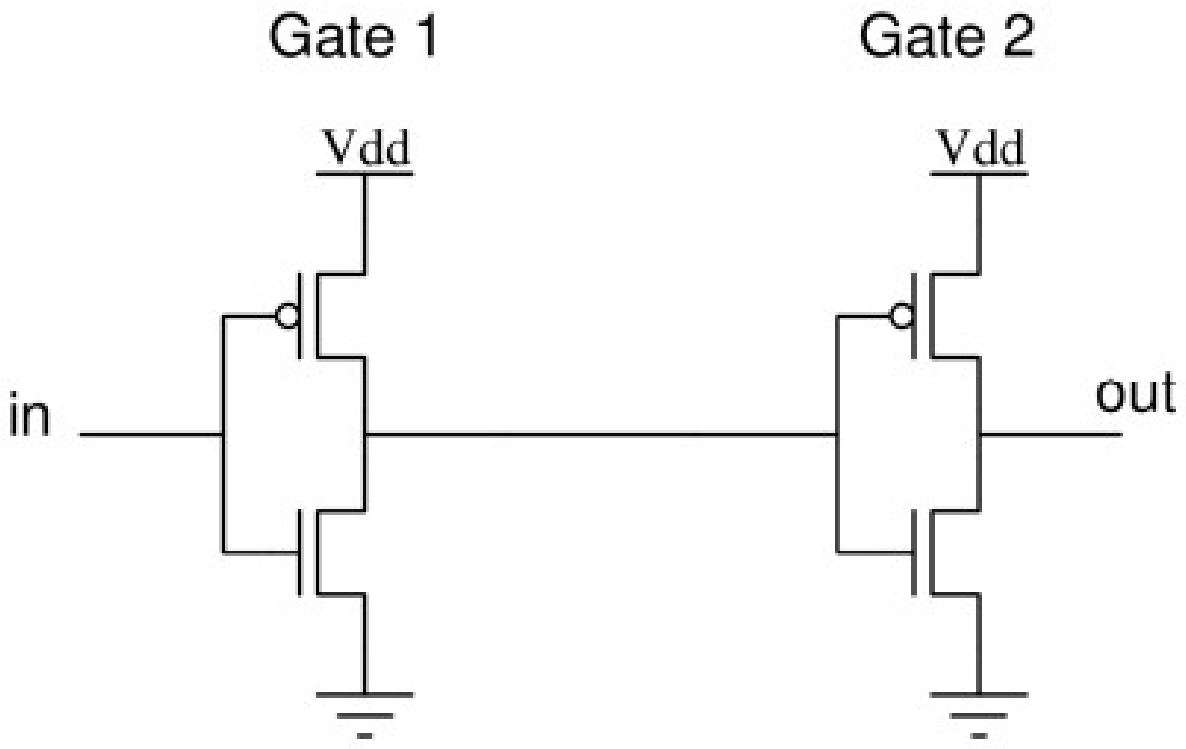
CMOS Inverter

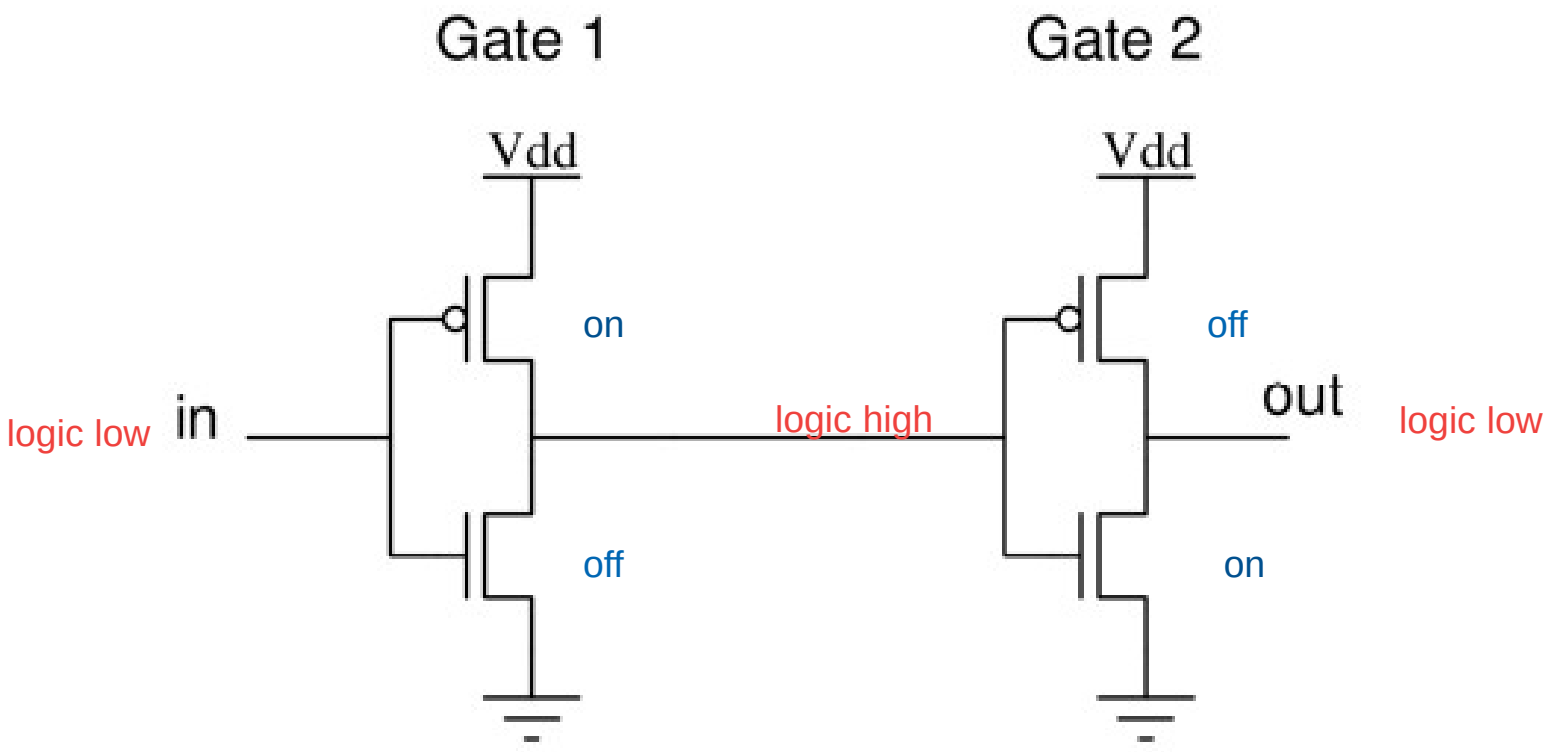


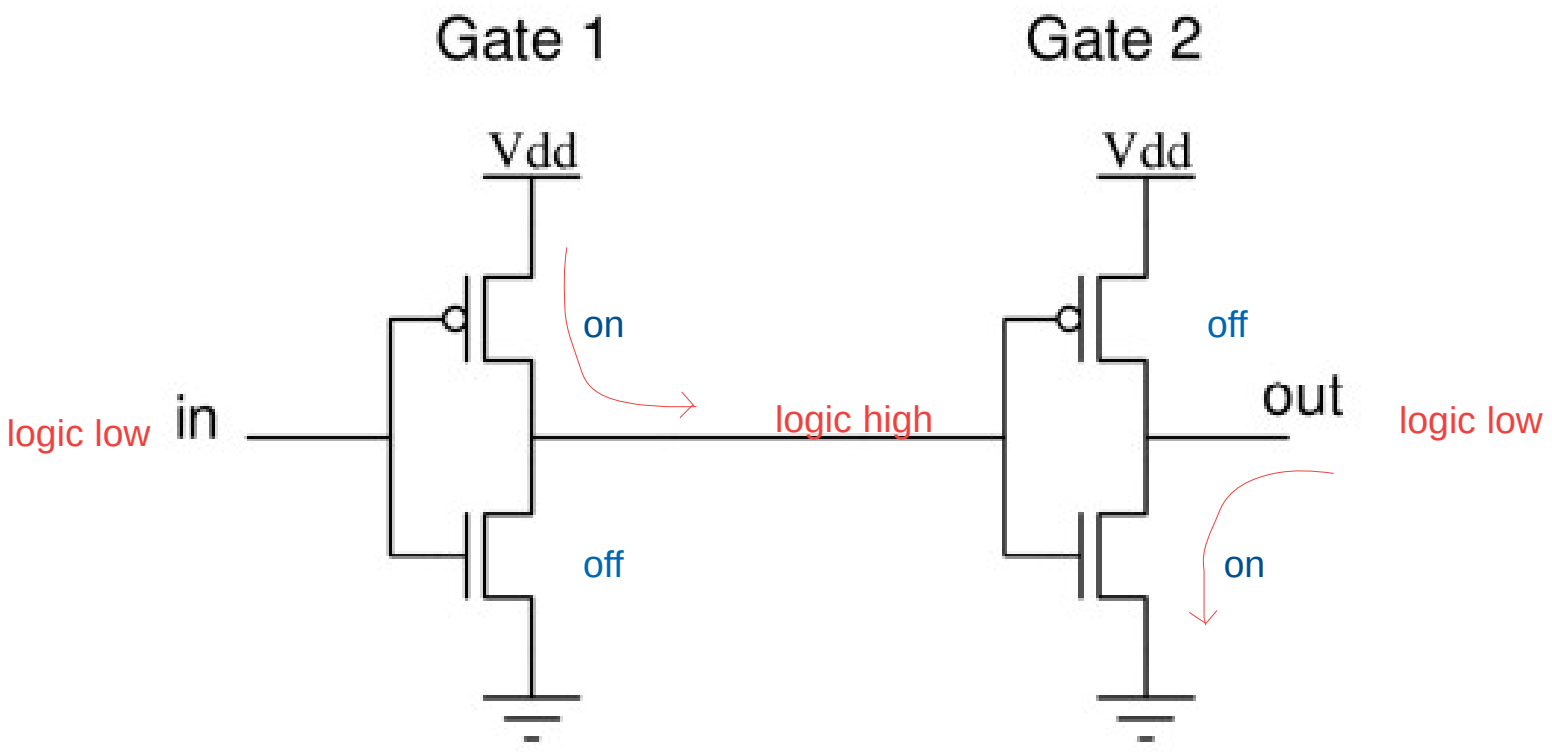


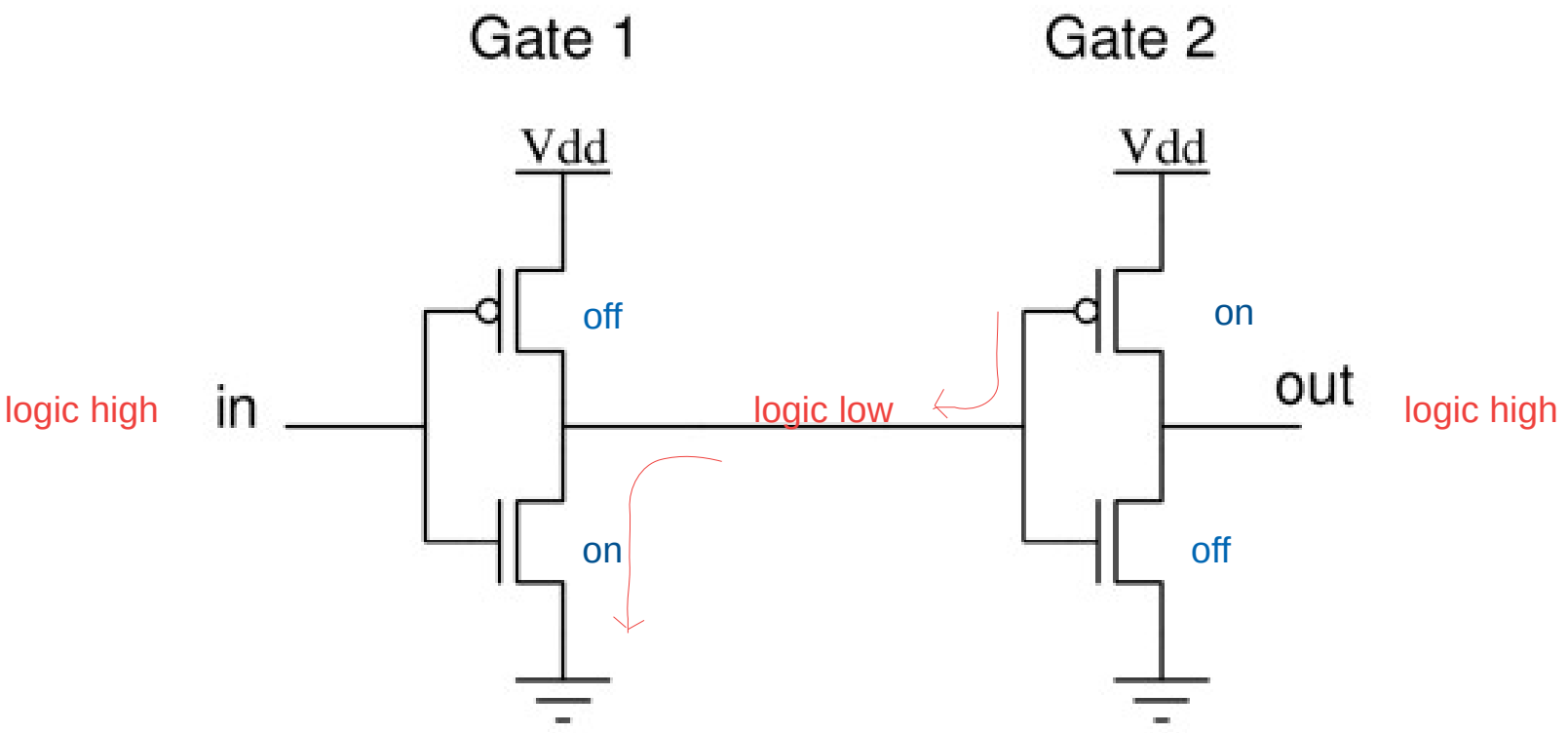

(a)
V_{DD} = +5.0 V
V_{IN} = L
V_{OUT} = H
(b)
V_{DD} = +5.0 V
V_{IN} = H
V_{OUT} = L

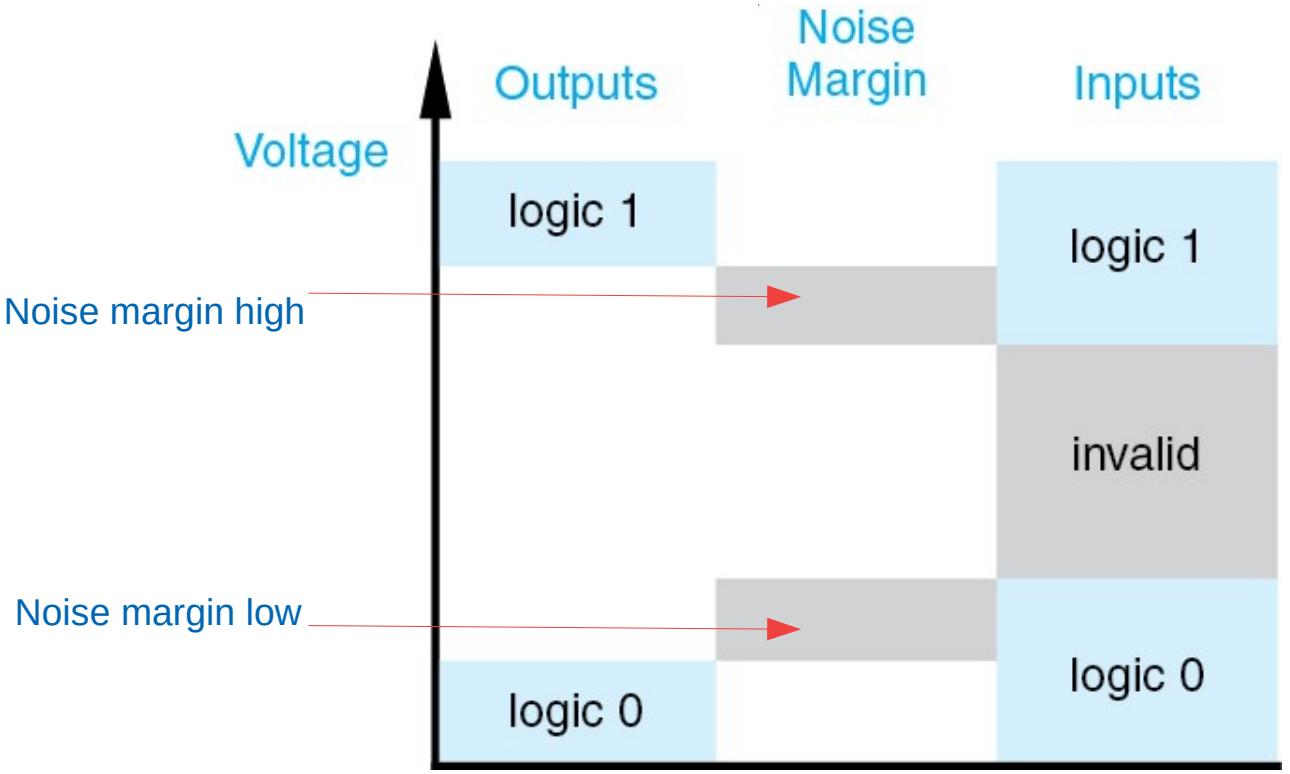

2-input NAND
Vdd
A in
p-mos
out
B in
n-mos


Gate 1
Gate 2
Vdd
Vdd
in
out


Gate 1
Gate 2
Vdd
Vdd
on
off
logic low
in
logic high
out
logic low
off
on


Gate 1
Gate 2
Vdd
Vdd
on
off
logic low
in
logic high
out
logic low
off
on


Gate 1
Gate 2
Vdd
Vdd
off
on
logic high
in
logic low
out
logic high
on
off



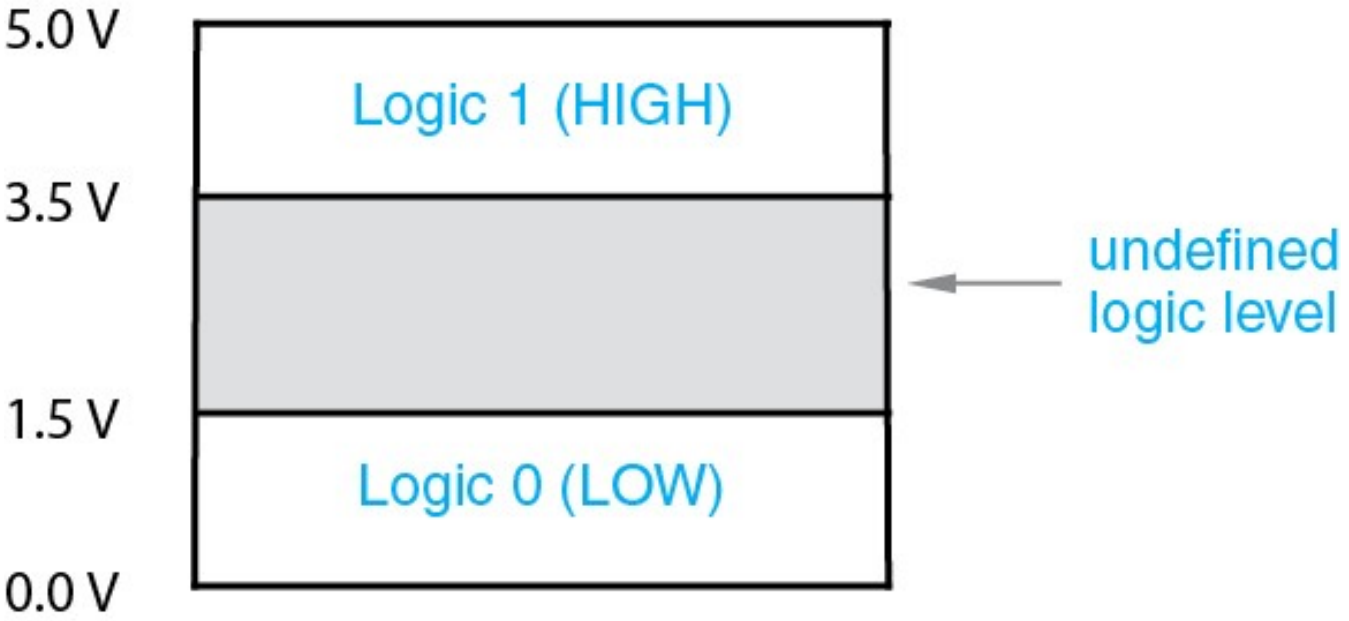
Noise margin high = (highstate Vout min) – (highstate Vin min)

$$NMH = V_{OH\ MIN} - V_{IH\ MIN}$$

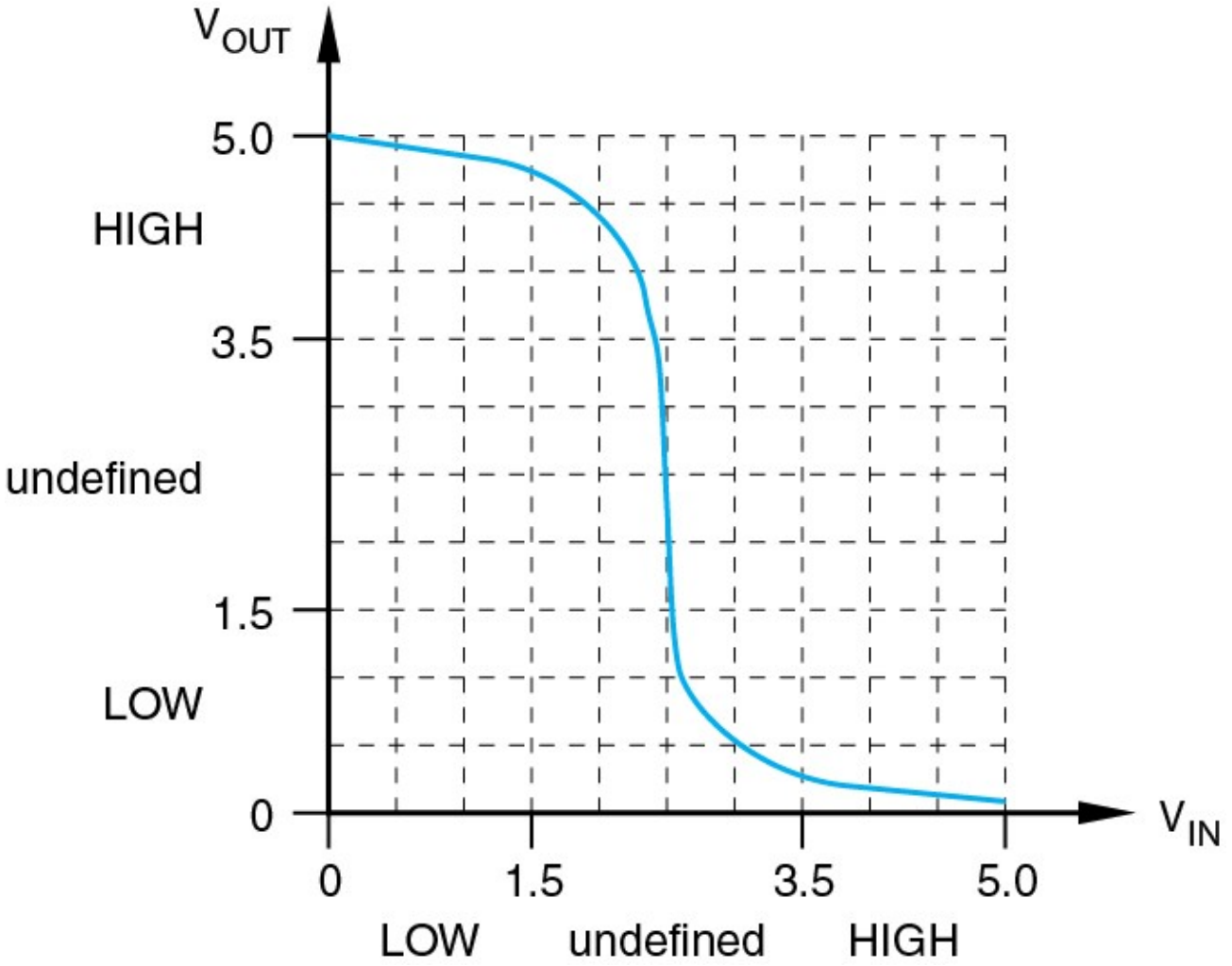
Noise margin low = (lowstate Vin max) – (lowstate Vout max)

$$NML = V_{IN\ MAX} – V_{OUT\ MAX}$$

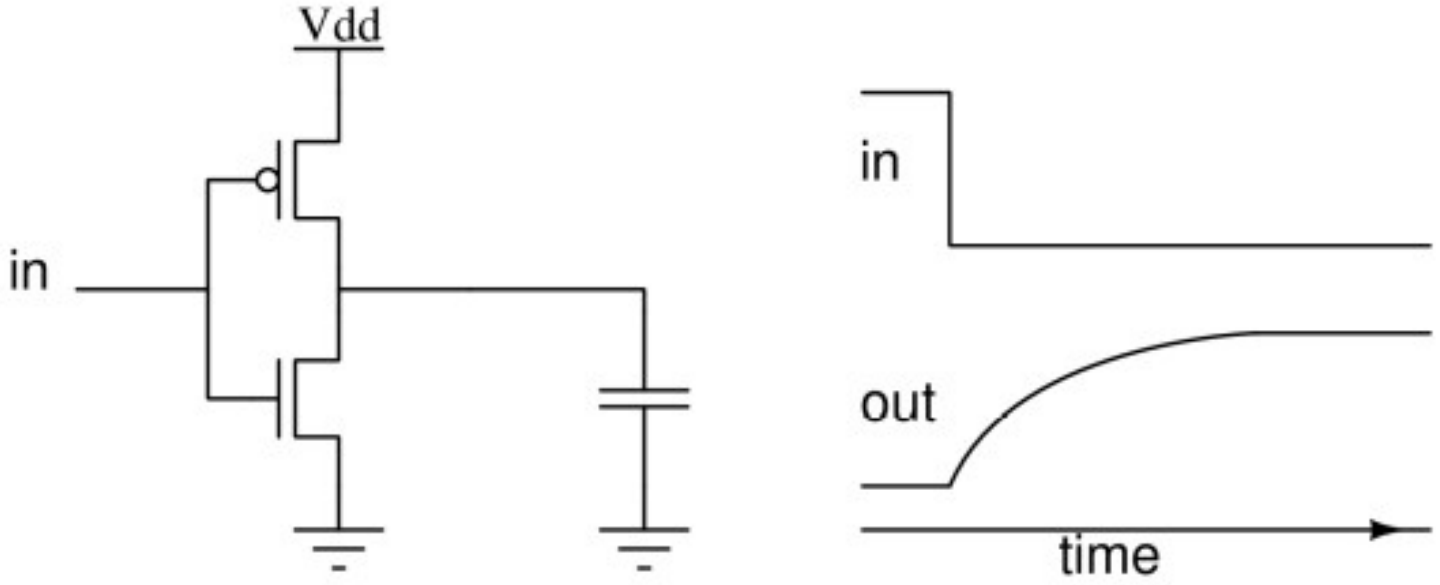
Typical 5v CMOS logic voltage levels



CMOS Inverter Vout vs Vin



CMOS Inverter with load



Example manufactures data for a 74HC00 CMOS NAND gate

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:

Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0\ V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

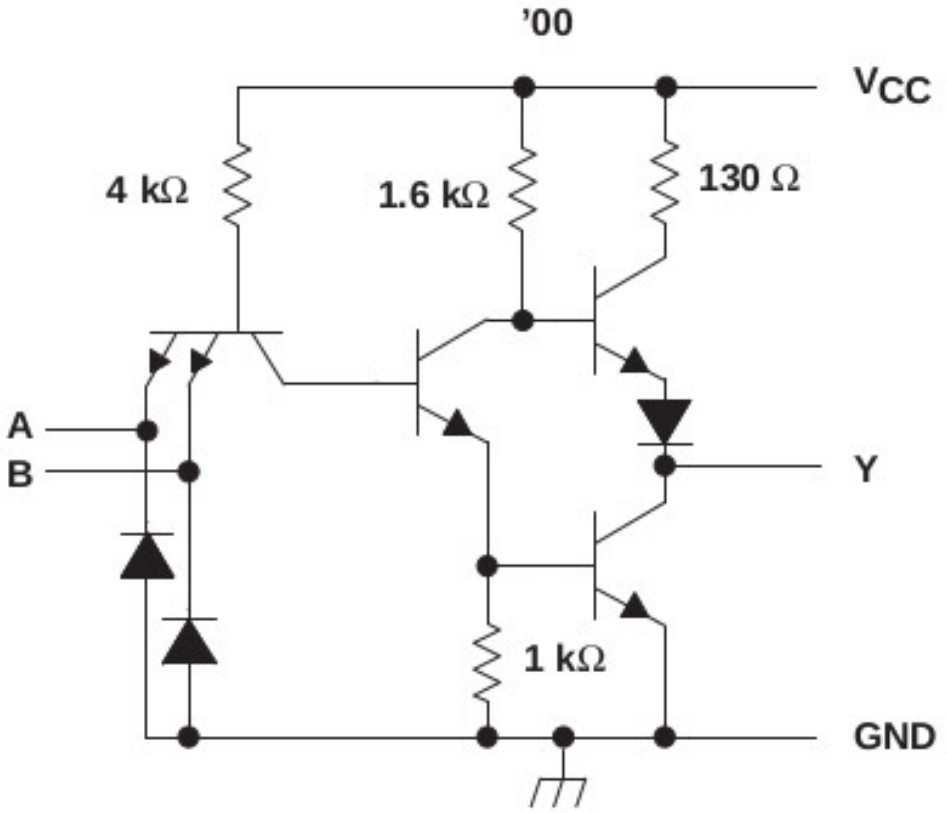
Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	–1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	–0.7	–1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	–35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20\ \mu$A	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min., $V_{IN} = V_{IH}$	$I_{OL} = 20\ \mu$A	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	V
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

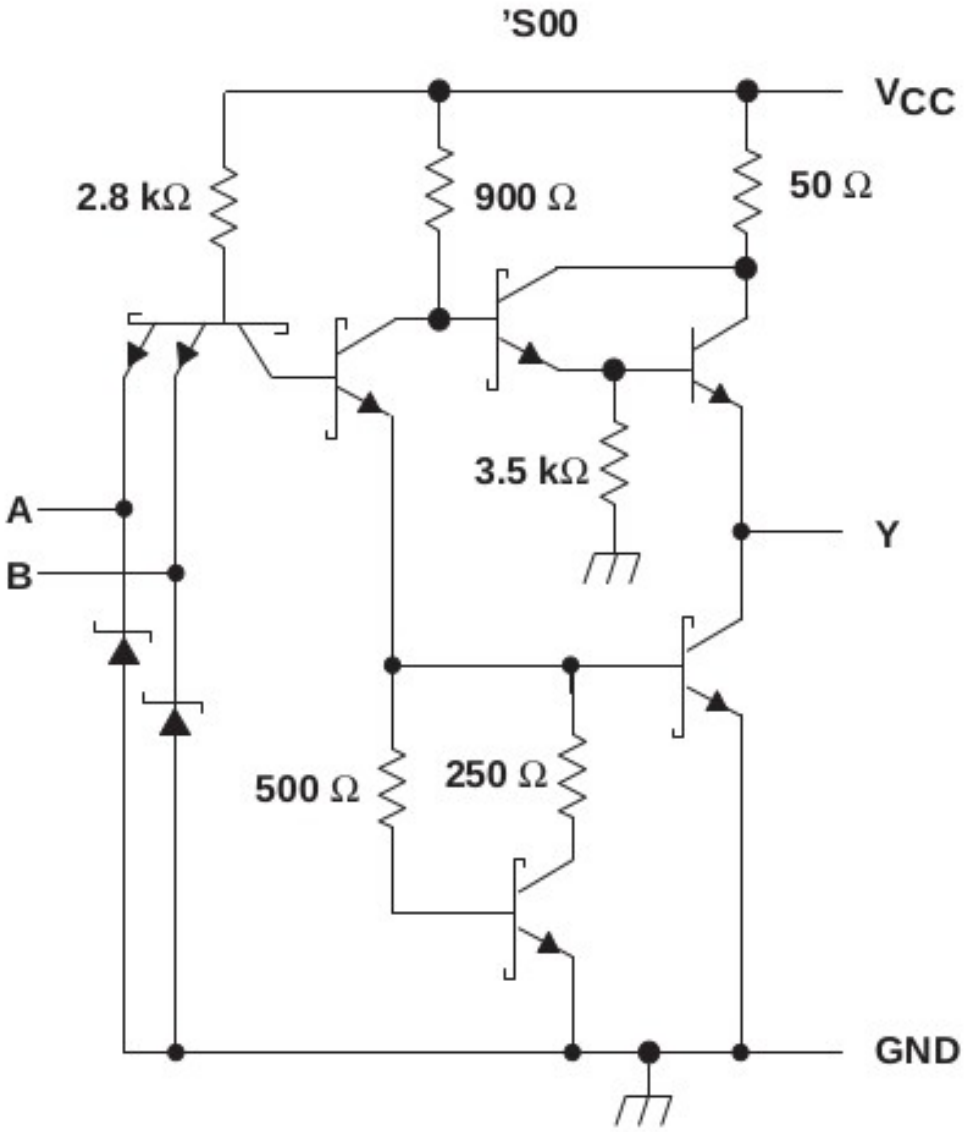
Sym.	Parameter[4]	Test Conditions	Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y	—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V	—	3	10	pF
C_{pd}	Power dissipation capacitance per gate	No load	—	22	—	pF

Transistor-Transistor Logic (TTL)

7400 NAND gate

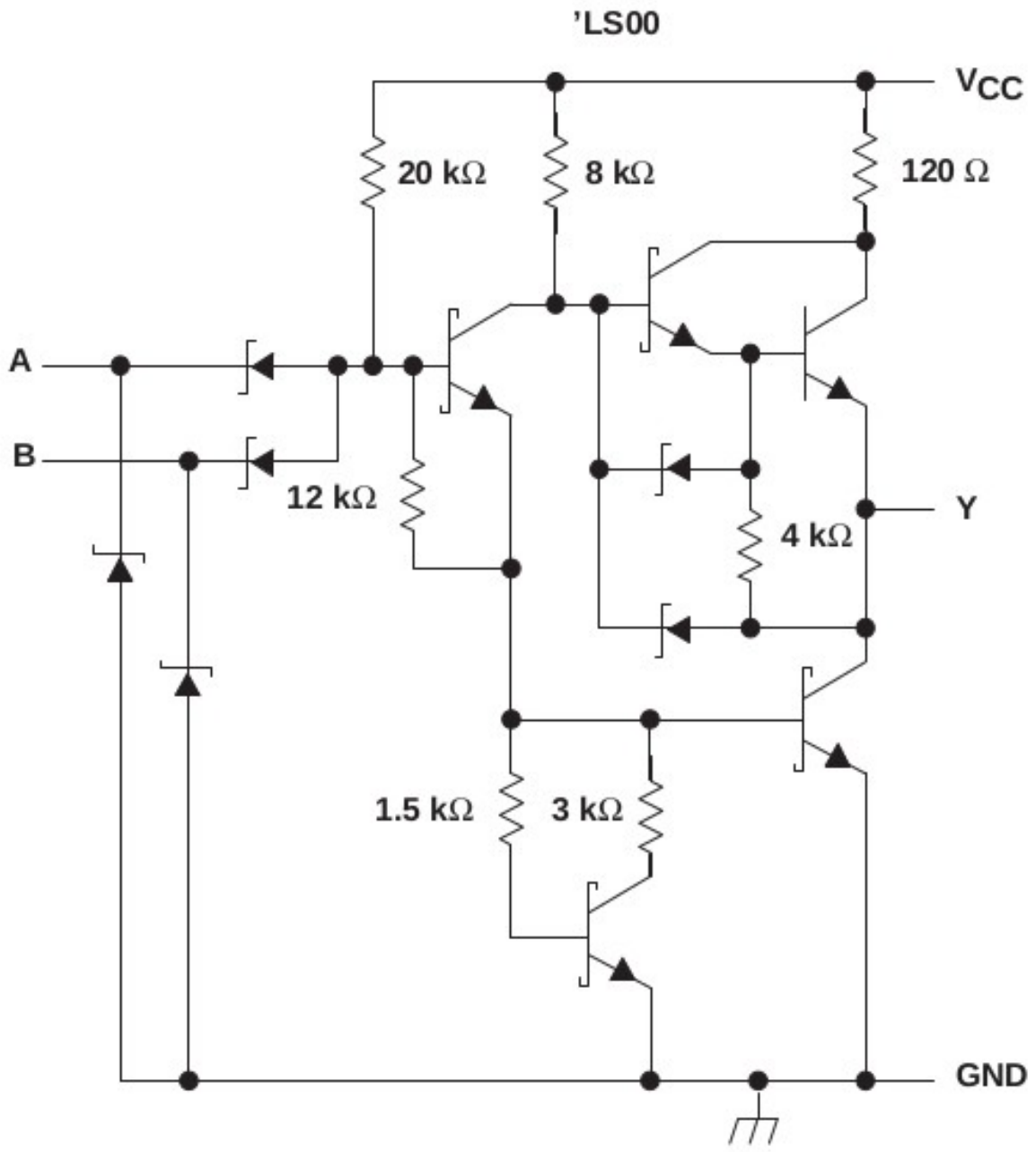


74S00 NAND gate
S = Schottky



74LS00 NAND gate

LS = Low power Schottky



recommended operating conditions (see Note 4)

		SN54LS00			SN74LS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

74LS00 NAND gate data

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

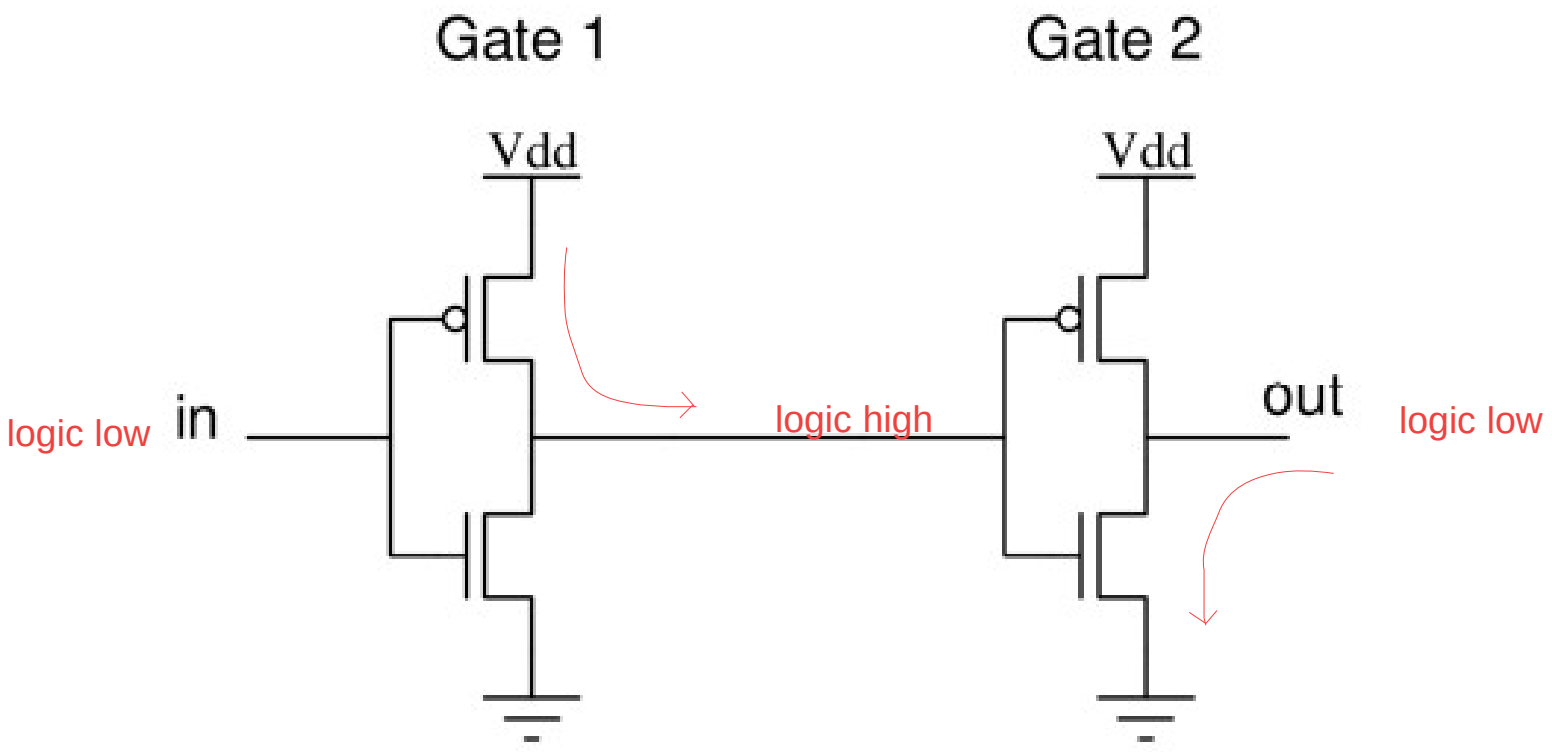
PARAMETER	TEST CONDITIONS†			SN54LS00			SN74LS00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

74LS00 NAND gate data

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS00 SN74LS00			UNIT
				MIN	TYP	MAX	
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	


Gate 1
Gate 2
Vdd
Vdd
logic low
in
logic high
out
logic low