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PRELIMINARY

Digilab 2E Reference Manual

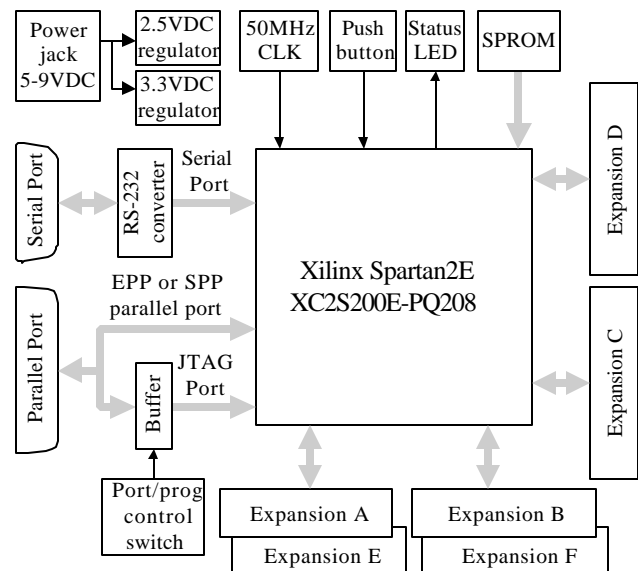
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Overview

The Digilab 2E (D2E) development board featuring the Xilinx Spartan 2E XC2S200E FPGA provides an inexpensive and expandable platform on which to design and implement digital circuits of all kinds. D2E board features include:

- A Xilinx XC2S200E FPGA;
- Dual on-board 1.5A power regulators (2.5V and 3.3V);
- A socketed 50MHz oscillator;
- An EPP-capable parallel port for JTAG-based FPGA programming and user data transfers;
- A 5-wire Rs-232 serial port;
- A status LED and pushbutton for basic I/O;
- Six 100-mil spaced, right-angle DIP socket 40-pin expansion connectors.

The D2E board has been designed specifically to work with the Xilinx ISE CAD tools, including the free WebPack tools available from the Xilinx website. Like other Spartan 2 boards in the Digilab family, the D2E board has been partitioned so that only the hardware required by a particular project need be purchased. Several existing peripheral boards



D2E circuit board block diagram

that mate with the expansion connectors are currently available (see www.digilentinc.com), and new boards are frequently added. The low-cost, standard expansion connectors allow new peripheral boards, including wire-wrap or manually soldered boards, to be quickly designed and used. The D2E board ships with a power supply and programming cable, so designs can be implemented immediately without the need for any additional hardware.

Functional description

The Digilab D2E board has been designed to offer a low-cost and minimal system for designers who need a flexible platform to gain exposure to the Spartan 2E device, or for those who need to prototype FPGA-based designs rapidly. The D2E board provides only the essential supporting devices for the Spartan 2E, and routes all available FPGA signals to standard expansion connectors. Included on the board are 2.5VDC and 3.3VDC regulators, a JTAG configuration circuit that uses a standard parallel cable, basic communication ports including an enhanced parallel port and 5-wire serial port, a 50MHz oscillator, and a pushbutton and LED for rudimentary I/O.

The D2E board has been designed to serve as a host for various peripheral boards. The expansion connectors on the D2E board mate with standard 40-pin, 100 mil spaced DIP headers available from any catalog distributor. Expansion connectors provide the unregulated supply voltage (VU), 3.3V, GND, and 37 FPGA signals to peripheral boards, so system designers can quickly develop application- specific peripheral boards. Digilent also produces a collection of expansion boards with commonly used devices. See the Digilent website (www.digilentinc.com) for a listing of currently available boards.

Table 1 shows all signals routed on the D2E board. These signals, and the circuits that they connect to, are described in the following sections.

| | |
|--------------------------------------|--|
| <u>Power Supplies</u> | |
| VU | Unregulated power supply voltage – depends on power supply used. Must be between 5VDC and 10VDC. Routed to regulators and expansion connectors only. |
| VDD33 | FPGA VCCO and VCC for all other devices, routed on PCB plane. 1.5A can be drawn with less than 20mV ripple (typical) |
| VDD25 | FPGA VCCINT routed on PCB plane |
| GND | System ground routed to all devices on PCB ground plane |
| <u>Programming and parallel port</u> | |
| PWE | EPP mode write enable signal (in to FPGA) |
| PD0-PD7 | Bi-directional data signals |
| PINT | Interrupt signal (out from FPGA) |
| PWT | EPP mode wait signal (out from FPGA) |
| PDS | EPP mode data strobe (in to FPGA) |
| PRS | Reset signal (in to FPGA) |
| PAS | EPP mode address strobe (in to FPGA) |
| <u>Serial port</u> | |
| RXD | Serial port receive data (in to FPGA) |
| TXD | Serial port send data (out from FPGA) |
| DSR | Serial port data set ready (out from FPGA) |
| CTS | Serial port clear to send (out from FPGA) |
| RST | Serial port request to send (in to FPGA) |
| <u>On board devices</u> | |
| BTN1 | User-controllable pushbutton input |
| LED1 | User-controllable status LED |
| CLK1 | CMOS oscillator connected to GCLK0 |
| <u>Expansion Connectors</u> | |
| A4-A40 | A bus signals connecting the A & E connectors to the FPGA |
| B4-B14 | B bus signals connecting the B & F connectors to the FPGA |
| C4-C40 | C bus signals connecting the C connector to the FPGA |
| D4-D40 | D bus signals connecting the D connector to the FPGA |

Table 1. D2E board signal definitions

Parallel port and FPGA configuration circuit

The Digilab 2E board uses a DB-25 parallel port connector to route JTAG programming signals from a host computer to the FPGA. This same connector also routes the computer’s parallel pins to the FPGA following the EPP port definition contained in the IEEE 1284 standard. A three-state buffer, controlled by a switch, determines whether the JTAG port or EPP port is enabled. With this circuit, the

FPGA can be configured using the JTAG protocol over the parallel cable. The same cable can then be used (after the switch is repositioned) to move data between the board and the host computer using the high-speed EPP protocol. A separate JTAG header is also provided so that a dedicated programming cable (like the Xilinx Parallel III cable) can be used.

The JTAG programming circuit follows the JTAG schematic available from Xilinx, so that the Digilab 2E board is fully compatible with all Xilinx programming tools. The EPP parallel port circuit follows the guidelines in the IEEE 1284 specification, and data rates approaching 2Mbytes/second can be achieved. JTAG and EPP connections are shown in the diagrams below.

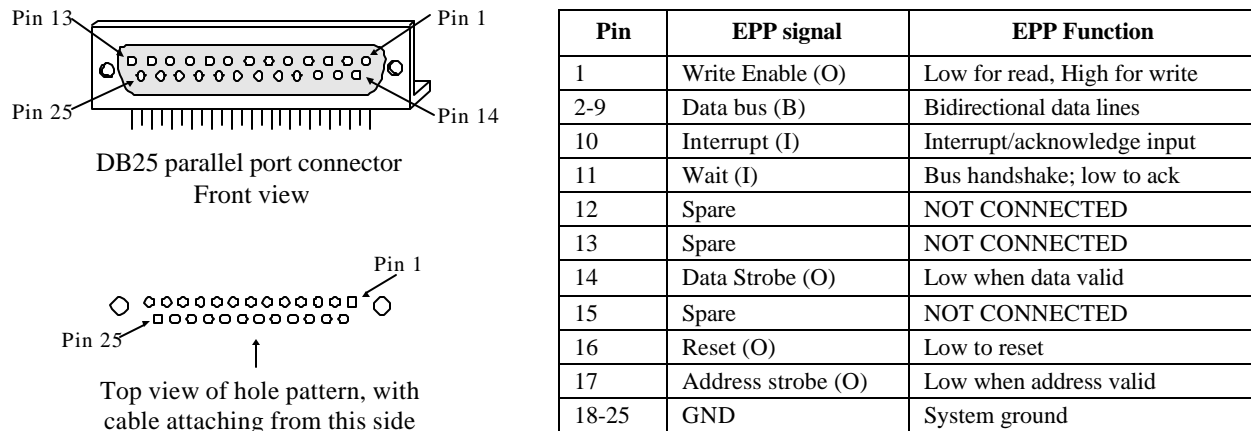


Figure 1. Parallel port connectors and signals

The D2E board directly supports JTAG and SPROM configuration. Hardware debugger configuration is supported indirectly. To configure the board from a computer using the JTAG mode, set switch 1 (SW1) in the JTAG position, and attach a power supply and programming cable. The power supply must be connected before the parallel cable, or the board may hang in a non-communicating state. The board will be auto-detected by the Xilinx JTAG programming software, and all normal JTAG operations will be available.

To configure the FPGA from an SPROM, load the programmed SPROM into the 8-pin ROM socket (labeled IC6), place SW1 in the PORT position, add jumpers to all mode pins, and apply power.

To configure the board using the hardware debugger protocol, a slight board modification is required – a jumper wire must be soldered to the non-VCC side of R45. Insert wire-wrap posts into the SPROM socket, attach the hardware debugger signals to the appropriate posts, and attach the PROG signal to the jumper wire attached to R45. The hardware debugger programming software will now automatically recognize the board, and hardware debugger programming can proceed as normal.

Programming circuit detail is shown below. Note that all parallel port signals are routed to the test header J12 for easy connection of test and measurement equipment.

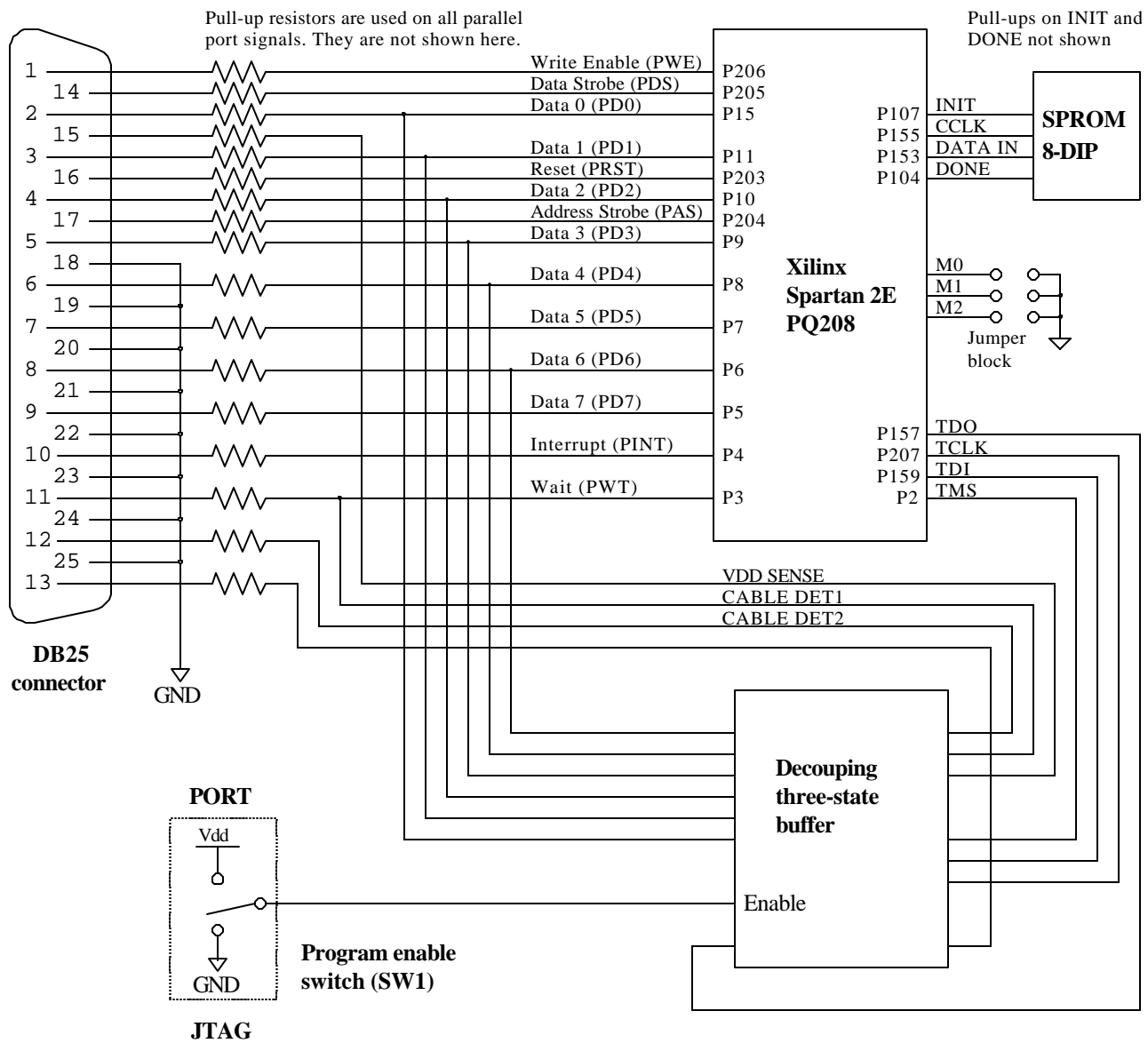


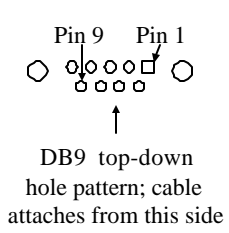
Figure 2. Parallel port and programming circuit schematic

Serial Port

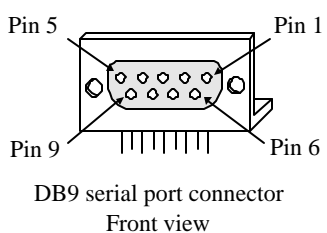
The D2E serial port uses a Maxim MAX3386E RS-232 voltage converter to generate the required RS-232 voltages. Five signals are connected through the RS-232 converter, allowing for partial hardware handshaking. The serial port pin definitions and circuit are shown below. The serial port is provided in part to support the Xilinx MicroBlaze embedded RSIC processor core available from the Xilinx website.

The two devices connected to either end of a serial cable are known as the Data Terminal Equipment (DTE) and the Data Communications Equipment (DCE). The DCE was originally conceived to be a modem, but now many devices connect to a computer as a DCE. A DTE device uses a male DB-9 connector, and a DCE device uses a female DB-9 connector. The DTE is considered the source of data, and the DCE the peripheral device. Two DTE devices can be connected via a serial cable only if lines

two and three are crossed – this is known as a null modem cable. A DTE and DCE device can be connected with a straight-through cable. The Digilab 2E board is configured as a DCE device.



DB9 top-down hole pattern; cable attaches from this side



DB9 serial port connector
Front view

Serial Port Pin Definitions

| Pin # | Name | Function | Direction | Connected |
|-------|------|---------------------|-----------|-----------|
| 1 | DCD | Data carrier detect | DCE → DTE | N |
| 2 | RXD | Received data | DCE → DTE | Y |
| 3 | TXD | Transmitted data | DCE ← DTE | Y |
| 4 | DTR | Data terminal ready | DCE ← DTE | N |
| 5 | SG | Signal ground | | Y |
| 6 | DSR | Data set ready | DCE → DTE | Y |
| 7 | RTS | Request to send | DCE ← DTE | Y |
| 8 | CTS | Clear to send | DCE → DTE | Y |
| 9 | RI | Ring Indicator | DCE → DTE | N |

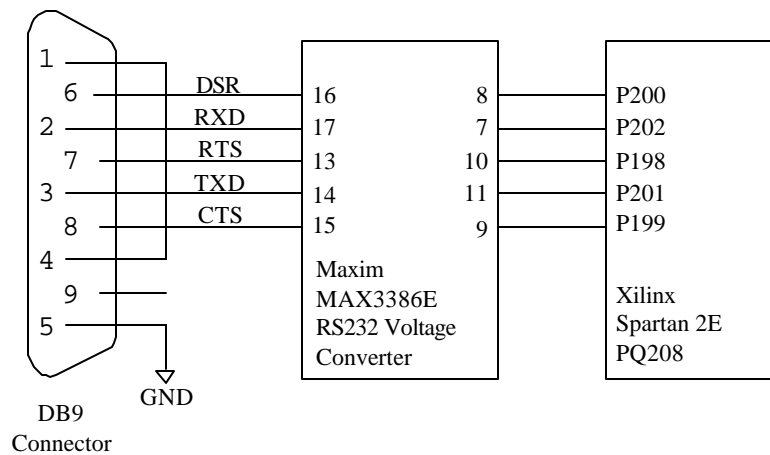


Figure 3. Serial port circuit schematic

Oscillator

The Digilab 2E uses a socketed half-size 8-pin DIP oscillator. The board ships with a 50MHz oscillator, allowing for system clocks from virtually DC to 200MHz (using the Spartan 2E DLL circuit and/or clock counter-dividers). Oscillators from 32KHz to 100MHz can easily be substituted, allowing for a wide range of clock frequencies. The oscillator, which is connected to the FPGA GCK0 input (P80), is bypassed with a 0.1uF capacitor and it is located as physically close to the FPGA as possible (trace length is about 10mm).

Power Supplies

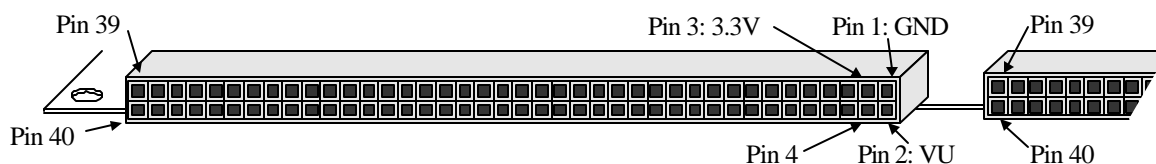
The Digilab 2E board uses two LM317 1.5A voltage regulators to produce 2.5VDC and 3.3VDC supplies. The regulator inputs are driven from an external DC power supply connected to the on-board 2.1mm center-positive power jack. The regulators have 10uF of input capacitance, 20uF of local output capacitance, and 10uF of regulation bypass capacitance. This allows the regulators to produce stable, low noise supplies using inexpensive power supplies, regardless of load (up to 1.5A). The regulator bodies are soldered to the board for improved thermal dissipation. DC supplies in the range of 5VDC to 10VDC may be used.

The Digilab 2E board uses a four layer PCB, with the inner layers dedicated to VCC and GND planes. Most of the VCC plane is at 3.3V, with an island under the FPGA at 2.5V. The FPGA and the other ICs on the board all have 0.1uF bypass capacitors placed as close as possible to the VCC pins.

Total board current is dependant on FPGA configuration, clock frequency, and external connections. In test circuits with roughly 50K gates routed, a 50MHz clock source, and a single expansion board attached (the DIO2 board), approximately 200mA +/- 30% of supply current is drawn from the 2.5V supply, and approximately 150mA +/- 50% is drawn from the 3.3V supply. These currents are strongly dependent on FPGA and peripheral board configurations.

All FPGA VCCO pins are connected to the 3.3V supply. If other VCCO voltages are required, please contact Digilent for information regarding various options (Digilent can be contacted through www.digilentinc.com).

Expansion connectors



The six expansion connectors labeled A-F use 100 mil spaced DIP headers. All six connectors have GND routed to pin 1, VU routed to pin 2, and 3.3V routed to pin 3. Pins 4-40 all route directly to the FPGA. The connectors are organized in pairs, with the A & B, C& D, and E & F pairs placed on the same board edge. Connectors A & B and E & F are routed in parallel, with pairs A & E and B & F sharing identical pin connections to the FPGA. Connectors C & D have all pins routed to separate FPGA pins. All connector pairs are separated by 400 mils, so any peripheral board can be placed in any connector (or pair of connectors).

The PQ208 package used on the D2E board allows 122 signals to be routed to the expansion connectors (the remaining 21 available signals are routed to the parallel and serial connectors). Connectors C and D are closest to the FPGA, and all C and D pins are connected to the closest available FPGA pins with the shortest possible route. Thus, the 74 FPGA signals routed to the C & D connectors will exhibit the least amount of signal delay, and data rates of up to 100MHz are attainable. The A & E connectors also route 37 FPGA signals, but with less favorable routes. Only 11 FPGA signals were left to route to the B & F connectors, so 26 pins on those connectors are not connected. Connector pin definitions follow.

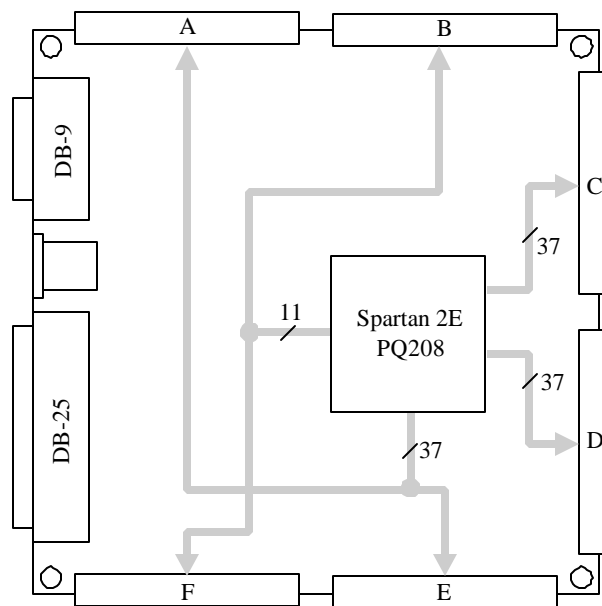


Figure 4. Expansion connector detail

Table 2. Digilab 2E Expansion Connector pinouts

| A&E connector | | |
|---------------|--------|----------|
| Pin | Signal | S-II pin |
| 1 | GND | - |
| 2 | VU | - |
| 3 | VDD33 | - |
| 4 | A4 | 68 |
| 5 | A5 | 64 |
| 6 | A6 | 63 |
| 7 | A7 | 62 |
| 8 | A8 | 61 |
| 9 | A9 | 60 |
| 10 | A10 | 59 |
| 11 | A11 | 58 |
| 12 | A12 | 57 |
| 13 | A13 | 56 |
| 14 | A14 | 55 |
| 15 | A15 | 49 |
| 16 | A16 | 48 |
| 17 | A17 | 47 |
| 18 | A18 | 46 |
| 19 | A19 | 45 |
| 20 | A20 | 44 |
| 21 | A21 | 43 |
| 22 | A22 | 42 |
| 23 | A23 | 41 |
| 24 | A24 | 40 |
| 25 | A25 | 36 |
| 26 | A26 | 35 |
| 27 | A27 | 34 |
| 28 | A28 | 33 |
| 29 | A29 | 31 |
| 30 | A30 | 30 |
| 31 | A31 | 29 |
| 32 | A32 | 27 |
| 33 | A33 | 24 |
| 34 | A34 | 23 |
| 35 | A35 | 22 |
| 36 | A36 | 21 |
| 37 | A37 | 20 |
| 38 | A38 | 18 |
| 39 | A39 | 17 |
| 40 | A40 | 16 |

| B&F connector | | |
|---------------|--------|----------|
| Pin | Signal | S-II pin |
| 1 | GND | - |
| 2 | VU | - |
| 3 | VDD33 | - |
| 4 | B4 | 194 |
| 5 | B5 | 193 |
| 6 | B6 | 192 |
| 7 | B7 | 191 |
| 8 | B8 | 189 |
| 9 | B9 | 188 |
| 10 | B10 | 187 |
| 11 | B11 | 185* |
| 12 | B12 | 182* |
| 13 | B13 | 181 |
| 14 | B14 | 180 |
| 15 | B15 | - |
| 16 | B16 | - |
| 17 | B17 | - |
| 18 | NC | - |
| 19 | NC | - |
| 20 | NC | - |
| 21 | NC | - |
| 22 | NC | - |
| 23 | NC | - |
| 24 | NC | - |
| 25 | NC | - |
| 26 | NC | - |
| 27 | NC | - |
| 28 | NC | - |
| 29 | NC | - |
| 30 | NC | - |
| 31 | NC | - |
| 32 | NC | - |
| 33 | NC | - |
| 34 | NC | - |
| 35 | NC | - |
| 36 | NC | - |
| 37 | NC | - |
| 38 | NC | - |
| 39 | NC | - |
| 40 | NC | - |

| C connector | | |
|-------------|--------|----------|
| Pin | Signal | S-II pin |
| 1 | GND | - |
| 2 | VU | - |
| 3 | VDD33 | - |
| 4 | C4 | 179 |
| 5 | C5 | 178 |
| 6 | C6 | 176 |
| 7 | C7 | 175 |
| 8 | C8 | 174 |
| 9 | C9 | 173 |
| 10 | C10 | 169 |
| 11 | C11 | 168 |
| 12 | C12 | 167 |
| 13 | C13 | 166 |
| 14 | C14 | 165 |
| 15 | C15 | 164 |
| 16 | C16 | 163 |
| 17 | C17 | 162 |
| 18 | C18 | 161 |
| 19 | C19 | 160 |
| 20 | C20 | 154 |
| 21 | C21 | 152 |
| 22 | C22 | 151 |
| 23 | C23 | 150 |
| 24 | C24 | 149 |
| 25 | C25 | 148 |
| 26 | C26 | 147 |
| 27 | C27 | 146 |
| 28 | C28 | 145 |
| 29 | C29 | 141 |
| 30 | C30 | 140 |
| 31 | C31 | 139 |
| 32 | C32 | 138 |
| 33 | C33 | 136 |
| 34 | C34 | 135 |
| 35 | C35 | 134 |
| 36 | C36 | 133 |
| 37 | C37 | 132 |
| 38 | C38 | 129 |
| 39 | C39 | 127 |
| 40 | C40 | 126 |

| D connector | | |
|-------------|--------|----------|
| Pin | Signal | S-II pin |
| 1 | GND | - |
| 2 | VU | - |
| 3 | VDD33 | - |
| 4 | D4 | 125 |
| 5 | D5 | 122 |
| 6 | D6 | 123 |
| 7 | D7 | 120 |
| 8 | D8 | 121 |
| 9 | D9 | 115 |
| 10 | D10 | 116 |
| 11 | D11 | 113 |
| 12 | D12 | 114 |
| 13 | D13 | 111 |
| 14 | D14 | 112 |
| 15 | D15 | 109 |
| 16 | D16 | 110 |
| 17 | D17 | 102 |
| 18 | D18 | 108 |
| 19 | D19 | 100 |
| 20 | D20 | 101 |
| 21 | D21 | 98 |
| 22 | D22 | 99 |
| 23 | D23 | 96 |
| 24 | D24 | 97 |
| 25 | D25 | 94 |
| 26 | D26 | 95 |
| 27 | D27 | 89 |
| 28 | D28 | 93 |
| 29 | D29 | 87 |
| 30 | D30 | 88 |
| 31 | D31 | 84 |
| 32 | D32 | 86 |
| 33 | D33 | 82 |
| 34 | D34 | 83 |
| 35 | D35 | 75 |
| 36 | D36 | 81 |
| 37 | D37 | 73 |
| 38 | D38 | 74 |
| 39 | D39 | 70 |
| 40 | D40 | 71 |

* uses GCLK pin

Pushbutton and LED

A single pushbutton and LED are provided on the board allowing basic status and control functions to be implemented without a peripheral board. As examples, the LED can be illuminated from a signal in the FPGA to verify that configuration has been successful, and the pushbutton can be used to provide a basic reset function independent of other inputs. The circuits are shown below.

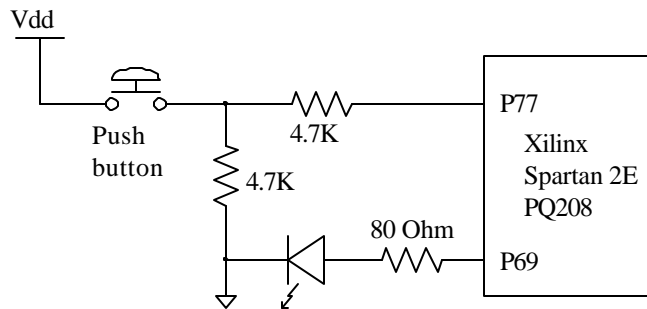


Figure 5. Pushbutton and LED detail

Spartan 2E FPGA

The block diagram of the Digilab 2E board shows all connections between the FPGA and the devices on the board. All FPGA pin connections are shown in the following table.

The Spartan device can be configured using the Xilinx JTAG tools and a parallel cable connecting the D2E board and the host computer. Note that a separate JTAG header that connects directly to the JTAG pins is also provided.

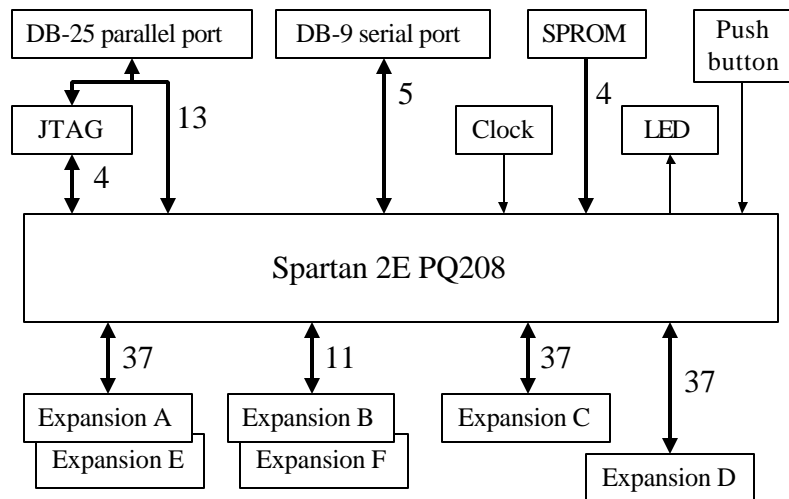


Figure 6. Spartan 2E connection detail

For further information on the Spartan FPGA, please see the Xilinx data sheets available at the Xilinx website (www.xilinx.com).

Table 3. Digilab 2E board Spartan 2E FPGA pinout

| Pin # | Function | Pin # | Function | Pin # | Function | Pin # | Function |
|-------|----------|-------|----------|-------|----------|-------|----------|
| 1 | GND | 53 | VCCO | 105 | VCCO | 157 | TDO |
| 2 | TMS | 54 | M2 | 106 | PROG | 158 | GND |
| 3 | PWT | 55 | A14 | 107 | INIT | 159 | TDI |
| 4 | PINT | 56 | A13 | 108 | D18 | 160 | C19 |
| 5 | PD7 | 57 | A12 | 109 | D15 | 161 | C18 |
| 6 | PD6 | 58 | A11 | 110 | D16 | 162 | C17 |
| 7 | PD5 | 59 | A10 | 111 | D13 | 163 | C16 |
| 8 | PD4 | 60 | A9 | 112 | D14 | 164 | C15 |
| 9 | PD3 | 61 | A8 | 113 | D12 | 165 | C14 |
| 10 | PD2 | 62 | A7 | 114 | D14 | 166 | C13 |
| 11 | PD1 | 63 | A6 | 115 | D9 | 167 | C12 |
| 12 | GND | 64 | A5 | 116 | D10 | 168 | C11 |
| 13 | VCCO | 65 | GND | 117 | GND | 169 | C10 |
| 14 | VCCINT | 66 | VCCO | 118 | VCCO | 170 | GND |
| 15 | PD0 | 67 | VCCINT | 119 | VCCINT | 171 | VCCO |
| 16 | A40 | 68 | A4 | 120 | D7 | 172 | VCCINT |
| 17 | A39 | 69 | LED1 | 121 | D8 | 173 | C9 |
| 18 | A38 | 70 | D39 | 122 | D5 | 174 | C8 |
| 19 | GND | 71 | D40 | 123 | D6 | 175 | C7 |
| 20 | A37 | 72 | GND | 124 | GND | 176 | C6 |
| 21 | A36 | 73 | D37 | 125 | D4 | 177 | GND |
| 22 | A35 | 74 | D38 | 126 | C40 | 178 | C5 |
| 23 | A34 | 75 | D35 | 127 | C39 | 179 | C4 |
| 24 | A33 | 76 | VCCINT | 128 | VCCINT | 180 | B14 |
| 25 | GND | 77 | BTN1* | 129 | C38 | 181 | B13 |
| 26 | VCCO | 78 | VCCO | 130 | VCCO | 182 | B12* |
| 27 | A32 | 79 | GND | 131 | GND | 183 | GND |
| 28 | VCCINT | 80 | CLK1* | 132 | C37 | 184 | VCCO |
| 29 | A31 | 81 | D36 | 133 | C36 | 185 | B11* |
| 30 | A30 | 82 | D33 | 134 | C35 | 186 | VCCINT |
| 31 | A29 | 83 | D34 | 135 | C34 | 187 | B10 |
| 32 | GND | 84 | D31 | 136 | C33 | 188 | B9 |
| 33 | A28 | 85 | GND | 137 | GND | 189 | B8 |
| 34 | A27 | 86 | D32 | 138 | C32 | 190 | GND |
| 35 | A26 | 87 | D29 | 139 | C31 | 191 | B7 |
| 36 | A25 | 88 | D30 | 140 | C30 | 192 | B6 |
| 37 | VCCINT | 89 | D27 | 141 | C29 | 193 | B5 |
| 38 | VCCO | 90 | VCCINT | 142 | VCCINT | 194 | B4 |
| 39 | GND | 91 | VCCO | 143 | VCCO | 195 | VCCINT |
| 40 | A24 | 92 | GND | 144 | GND | 196 | VCCO |
| 41 | A23 | 93 | D28 | 145 | C28 | 197 | GND |
| 42 | A22 | 94 | D25 | 146 | C27 | 198 | RTS |
| 43 | A21 | 95 | D26 | 147 | C26 | 199 | CTS |
| 44 | A20 | 96 | D23 | 148 | C25 | 200 | DSR |
| 45 | A19 | 97 | D24 | 149 | C24 | 201 | TXD |
| 46 | A18 | 98 | D21 | 150 | C23 | 202 | RXD |
| 47 | A17 | 99 | D22 | 151 | C22 | 203 | PRS |
| 48 | A16 | 100 | D19 | 152 | C21 | 204 | PAS |
| 49 | A15 | 101 | D20 | 153 | DIN | 205 | PDS |
| 50 | M1 | 102 | D17 | 154 | C20 | 206 | PWE |
| 51 | GND | 103 | GND | 155 | CCLK | 207 | TCK |
| 52 | MO | 104 | DONE | 156 | VCCO | 208 | VCCO |

* uses GCLK pin