HW #8 - Create a block diagram of a circuit to do the following:

Problem Statement

1) Design an 8-bit serial data transmitter and implement on a WWU FPGA3 board. Assume a three signal interface will be used to transfer data to a receiving circuit: a data line, data clock, and data start signal (see figure 1). The transmitter will have an 8-bit data input (sw0 to sw7) , a Go signal (sw16), and system clock. When the Go signal is asserted, a byte will be read from sw0-7 and placed into transmit memory, and then transmission will begin. Bit 0 will be transmitted first, Bit 1 next, etc. Transmitter outputs will be as follows:

   data clock - extout0
   start signal - extout1
   data line - extout2

   The data clock rate will be 1.0 MHz (although for debugging it may be helpful to use a slower clock).

2) Design an 8-bit serial data receiver for the three wire interface and implement. Assign incoming data to these ports:

   data clock - extin0
   start signal - extin1
   data line - extin2

   Received data is to be displayed on 8 LEDs, LED 0-7. Recall that data bit reception will be "clocked" by the transmitted data clock, not by a clock local to the reciever..

Use a scope or logic analyzer to display the bit clock, data start signal, and serial bit stream simultaneously.

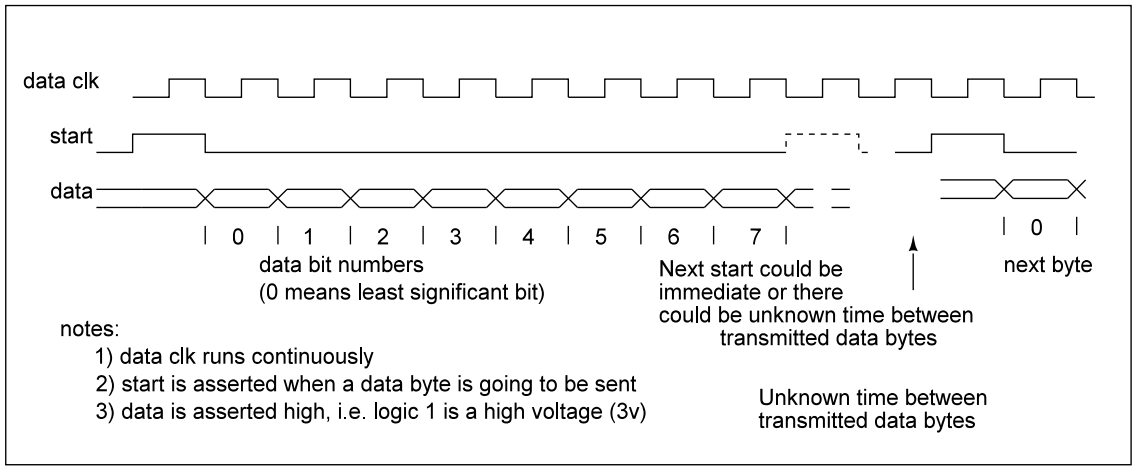

Figure 1 - timing diagram