Note regarding Lab 1 write up

In the instructions for lab 1 you are asked to determine how fast you can clock the state machine you designed. This you will determine in two ways. First, empirically using a signal generator to clock the state machine. While observing the Sync and Wave outputs on a scope, increase the signal generator frequency until you observe failure. As clock frequency increases the waveforms will become distorted or "noisy". Failure could mean that at some frequency the waveform is too distorted to be interpreted per the problem definition Or at some frequency the period of the waveforms may suddenly increase as you increase frequency. This indicates that the state machine cannot run as fast as the clock is trying to make it and that the new next state is not generated fast enough to be captured on the next clock tick. An extra clock tick goes by and the period of the output waveform suddenly is longer than at a slightly lower frequency.

The second way to determine how fast the state machine can be clocked is by calculation. It takes time for a signal to propagate through a logic gate. This is called propagation delay t_{pd}. I mentioned this briefly in class but we need to explore it further. Visualize the signal path in the synchronous state machine as transitions are made state to state. The sequence goes like this:
-    A rising clock edge occurs and the logic signal on the D input of the state bit travels (propagates) to the output of the flip-flop creating a new present state.
-    The new present state propagates through various gates in the next state forming logic to create a new next state that becomes new input data to the flip-flops.
-    Data input to a flip-flop needs to be present ahead of the clock edge that causes the flip-flop to read new data (typically the rising edge). This is called set-up time t_{su}.

The figure below shows the signal flow timing in a state machine.
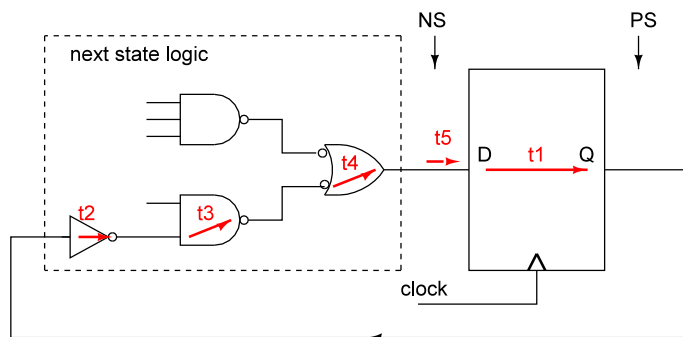
t1 - propagation time from clock edge to new data at Q
t2 - propagation time
t3 - propatation time
t4 - propagation time
t5 - flip-flop set up time
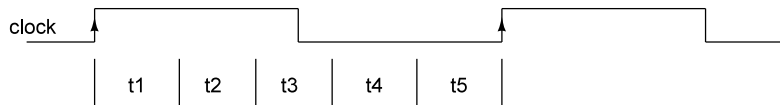
t1 + t2 + t3 + t4 + t5 must be less than the clock period for proper operation. Thus the fastest clock speed is the reciprocal of t1 + t2 + t3 + t4 + t5.

On the class web page are data sheets for the 74HCxx series of logic parts that we used for this lab. You need to look at the data sheets and find values for the various propagation and set-up times. For example on page 3 of the 74HC00 data sheet you will find a table and in that table a value for propagation time t_p. You will notice that the propagation time varies depending on power supply voltage (use the 4.5v value if powering with 5v). There are also typical values at 25 degrees and max values given for both 54HC00 and 74HC00 parts. Max values allow for operating temperature over its stated range and statistical variation due to manufacturing variation. (the 54HCxx parts are military grade parts while 74HCxx parts are considered commercial grade parts)

You can use the typical propagation times for this lab.

On page 4 of the 74HC74 data sheet are found values for propagation clock edge to Q output and data set-up time. In addition, there is a maximum clock rate value.

In your lab report or lab notes you should show calculation of the maximum clock frequency based on data sheet values.

I encourage you to spend some time looking at the data sheets. You need to master reading them.