Lab Exercise #5

Objective

The objective of this lab is to continue learning VHDL by designing and implementing a circuit that multiplies two 4-bit numbers and displays the result in decimal on a 7-segment display..

References

On-line from the class webpage are manuals for the Xilinx software and hardware.

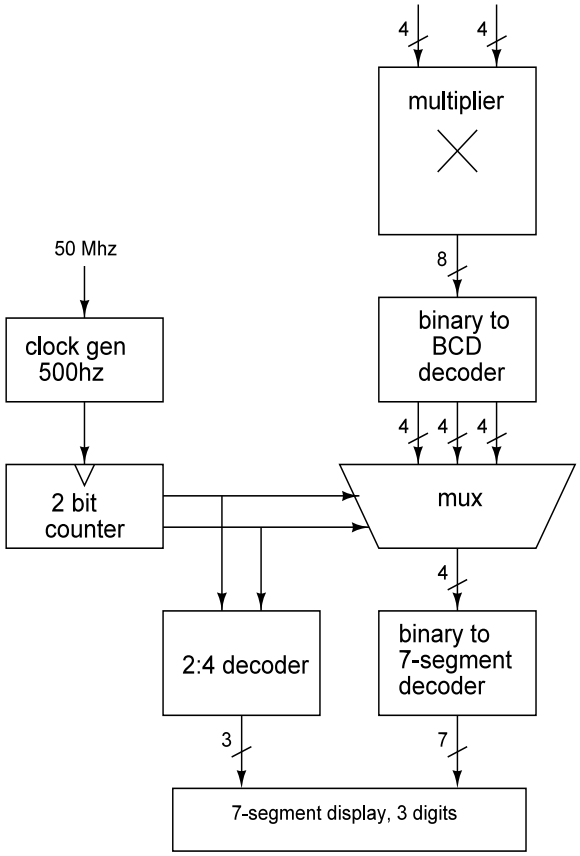
Design Flow

The general design flow we are using is described below.

- Initial design (block diagram in particular)
- Describe the design using VHDL
- Synthesize using Xilinx software
- Download to FPGA board using Impact
- Verify operation. Iterate as needed.

Problem Statement

Create a lab 5 project that implements the block diagram below:



Design Process

Before writing any VHDL create a neat block diagram (pencil/paper or electronic tool) showing the circuit functional blocks you need to create and the interconnections between them (mostly done for this lab). When writing the VHDL description for this block diagram you should be able to easily identify the statements that relate to each block in the diagram (i.e. put in comments). Some blocks may be defined as components and be instantiated into the top level architecture for convenience or general organization of the design, but you don't have to create separate components for every block You can have multiple processes and assignment statements in your top level source file. Use dividing lines and comments to make it easy to identify blocks and components.

FPGA Pinout Definition

(use a constraint file)

Input Connections

Master clock (50Mhz)
Switches 7 to 4 are one 4-bit number and switches 3 to 0 are the second.

Output Connectsions

Cathodes 0 to 6 is the data out
Cathode 7 (decimal point) is not used and can be connected to Vdd
Anodes 0 to 2 are sequentially turned on to multiplex data to 3 digits
Anodes 3 and 4 are not used and can be connected to Vdd.

To Turn In

A report is required from each person and consists of:

- a one page synopsis of what you did in lab, procedures followed, results, and problems if any.
- block diagram
- a copy of the VHDL definition(s)
- statistics: number of slice F/Flops used, # of occupied slices, # of slices containing unrelated logic, number of bonded IOBs, the number of BUFGMUXs, and average fanout of non-clock nets.