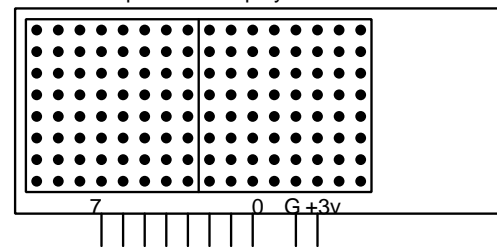


FPGA board

Top view of display circuit board



- Notes:
- 1) To send clock to the A/D converter use extout8
Use an extin port to send CE to the A/D (although named input, the inputs can be used for output)
 - 2) 29 bits, including the sign bit, are shown as input to the "magic" block. This would be the number for a 32 tap filter. If you are using 16 taps there will be 28 bits and you could concatenate a fixed zero as the least significant bit going into the magic block. Or modify the magic block description.
 - 3) For one FIR filter output, as shown above, one column of 8 LEDs will be used. As shown, column zero.

Lab 8 display details

L.Aamodt		12/11/16
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