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# FPGA1 constraint file, for use with SWLED11 interface card
# Ralph Stirling 2010-10-21

NET "clk"       LOC="P89";   # 50MHz clock oscillator
NET "tx"        LOC="P53";   # UART transmit
NET "rx"        LOC="P69";   # UART receive

# Header J1 (ref des on SWLED11 board, not FPGA1 board)

NET "led<12>"         LOC="P98";             #J1-3
NET "led<13>"         LOC="P95";             #J1-4
NET "led<14>"         LOC="P94";             #J1-5
NET "led<15>"         LOC="P92";             #J1-6
NET "led<16>"         LOC="P91";             #J1-7
NET "extin<0>"        LOC="P90" | PULLDOWN;  #J1-8
NET "extin<1>"        LOC="P86" | PULLDOWN;  #J1-9
NET "extin<2>"        LOC="P85" | PULLDOWN;  #J1-10
NET "extin<3>"        LOC="P84" | PULLDOWN;  #J1-11
NET "extin<4>"        LOC="P83" | PULLDOWN;  #J1-12
NET "extin<5>"        LOC="P79" | PULLDOWN;  #J1-13
NET "extin<6>"        LOC="P78" | PULLDOWN;  #J1-14
NET "extin<7>"        LOC="P88" | PULLDOWN;  #J1-18
NET "extout<0>"       LOC="P71";             #J1-21
NET "extout<1>"       LOC="P70";             #J1-22
NET "extout<2>"       LOC="P68";             #J1-23
NET "extout<3>"       LOC="P67";             #J1-24
NET "extout<4>"       LOC="P66";             #J1-25
NET "extout<5>"       LOC="P65";             #J1-26
NET "extout<6>"       LOC="P63";             #J1-27
NET "extout<7>"       LOC="P62";             #J1-28
NET "extout<8>"       LOC="P61";             #J1-29
NET "led<5>"          LOC="P60";             #J1-30  jumper to J2-27
NET "led<11>"         LOC="P58";             #J1-31  jumper to J2-36
NET "J1<32>"          LOC="P57";             #J1-32

# Header J2

NET "sw<0>"           LOC="P2";    #J2-3
NET "sw<1>"           LOC="P3";    #J2-4
NET "sw<2>"           LOC="P4";    #J2-5
NET "sw<3>"           LOC="P5";    #J2-6
NET "sw<4>"           LOC="P9";    #J2-7
NET "sw<5>"           LOC="P10";   #J2-8
NET "sw<6>"           LOC="P11";   #J2-9
NET "sw<7>"           LOC="P12";   #J2-10
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NET "sw<8>"         LOC="P15";   #J2-11
NET "sw<10>"        LOC="P16";   #J2-12
NET "sw<12>"        LOC="P17";   #J2-13
NET "sw<14>"        LOC="P18";   #J2-14
NET "sw<9>"         LOC="P22";   #J2-15
NET "sw<11>"        LOC="P23";   #J2-16
NET "sw<13>"        LOC="P24";   #J2-17
NET "sw<15>"        LOC="P13";   #J2-18
NET "sw<16>"        LOC="P27";   #J2-21
NET "led<0>"        LOC="P32";   #J2-22
NET "led<1>"        LOC="P33";   #J2-23
NET "led<2>"        LOC="P34";   #J2-24
NET "led<3>"        LOC="P35";   #J2-25
NET "led<4>"        LOC="P36";   #J2-26
NET "J2<27>"        LOC="P38";   #J2-27 input only
NET "led<6>"        LOC="P40";   #J2-28
NET "led<7>"        LOC="P41";   #J2-29
NET "led<8>"        LOC="P47";   #J2-30
NET "led<9>"        LOC="P48";   #J2-31
NET "led<10>"       LOC="P49";   #J2-32
NET "J2<36>"        LOC="P30";   #J2-36 input only
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Notes:

P89 is a global clock input (GCLK9)

P83, P84, P85, P86, P88, P90 can connect to global clocks (4,5,6,7,8,10 respectively)