ENGR 434 - VLSI Design 2019

rev 1

| Date | | Topic | Reading |
|---|---|---|---|
| M | April 1 | Overview of IC design | |
| W | 3 | Introduction to CMOS circuits | Chapter 1 |
| | | MOS transistors | 1.3 |
| | | CMOS Logic | 1.4 |
| | | CMOS Fabrication & Layout | 1.5 |
| F | 5 | Introduction to system design | |
| | | Design Partitioning | 1.6 |
| | | Example: simple MIPS uP | 1.7 |
| | | Logic Design | 1.8 |
| | | Circuit Design | 1.9 |
| | | Physical Design | 1.10 |
| | | Design Verification | 1.11 |
| M | 8 | MOS Transistor Theory | Chapter 2 |
| | | nMOS and pMOS | 2.1 |
| | | channel enhancement | |
| | | threshold voltage | |
| | | MOS current-voltage characteristics | 2.2 |
| | | MOS capacitances | 2.3.1 |
| W | 10 | MOS transistor theory continued | |
| | | Nonideal I-V Effects | 2.4 |
| | | Mobility and Velocity | 2.4.1 |
| | | Channel Length Modulation | 2.4.2 |
| | | Threshold voltage effects | 2.4.3 |
| | | Leakage | 2.4.4 |
| | | Temperature Dependence | 2.4.5 |
| | | Geometry Dependence | 2.4.6 |
| | | Nonideal summary | 2.4.7 |
| F | 12 | MOS theory cont. - DC transfer characteristics | |
| | | CMOS inverter | 2.5.1 |
| | | Beta ratios | 2.5.2 |
| | | Noise Margin | 2.5.3 |
| | | Pass transistor characteristics | 2.5.4 |
| . | | Delay | 4.1-4.3 |
| | | Delay Introduction | 4.1 |
| | | Transient response | 4.2 |
| | | RC delay model | 4.3 |
| | | Elmore delay | 4.3.5 |
| M | 15 | CMOS Processing Technology | Chapter 3 |
| | | Overview; | 3.1 |
| | | Wafer creation | 3.2.1 |
| | | Photolithography | 3.2.2 |

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|---|---|---|---|
| | | Well and channel formation | 3.2.3 |
| | | N-well, P-well, twin-well processes | |
| | | Silicon dioxide | 3.2.4 |
| | | Isolation | 3.2.5 |
| | | Gate oxide | 3.2.6 |
| | | Gate and source/drain formations | 3.2.7 |
| | | Contacts and metalization | 3.2.8 |
| | | Passivation | 3.2.9 |
| W | 17 | Layout Design Rules | 3.3 |
| | | Well rules | 3.3.1.1 |
| | | Transistor rules | 3.3.1.2 |
| | | Contact rules | 3.3.1.3 |
| | | Metal rules | 3.3.1.4 |
| | | Via rules | 3.3.1.5 |
| | | Other rules | 3.3.1.6 |
| F | 19 | Logical Effort | Chapter 4 |
| | | Linear delay model | 4.4 |
| | | Logical effort | 4.4.1 |
| | | Parasitic delay | 4.4.2 |
| | | Delay in a logic gate | 4.4.3 |
| | | Drive | 4.4.4 |
| | | Logical effort of paths | 4.5 |
| | | Delay in multistage networks | 4.5.1 |
| | | Choosing the best # of stages | 4.5.2 |
| | | Summary and observations | 4.5.4 |
| M | 22 | Combinational circuit design | Chapter 9 |
| | | Introduction | 9.1 |
| | | Static CMOS | 9.2.1 |
| | | Bubble pushing | 9.2.1.1 |
| | | Compound gates | 9.2.1.2 |
| | | Input ordering delay effect | 9.2.1.3 |
| | | Asymmetric gates | 9.2.1.4 |
| | | Skewed gates | 9.2.1.5 |
| | | P/N ratios | 9.2.1.6 |
| W | 24 | Combinational circuit design continued | |
| | | Pass-transistor circuits | 9.2.5 |
| | | CMOS transmission gates | 9.2.5.1 |
| | | Circuit pitfalls | 9.3 |
| | | Threshold drops | 9.3.1 |
| | | Leakage | 9.3.3 |
| | | Power supply noise | 9.3.5 |
| | | Hot spots | 9.3.6 |
| | | Minority carrier injection | 9.3.7 |
| | | Diffusion input noise sensitivity | 9.3.9 |
| | | Process sensitivity | 9.3.10 |
| F | 26 | Exam1 | |

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| M | 29 | Sequential circuit design | Chapter 10 |
| | | Sequencing static circuits | 10.2 |
| | | Sequencing methods | 10.2.1 |
| | | Max-delay constraints | 10.2.2 |
| | | Min-delay constraints | 10.2.3 |
| | | Clock skew | 10.2.5 |
| | | Design of Latches & Flip/flops | 10.3 |
| | | Conventional CMOS latches | 10.3.1 |
| | | Conventional CMOS flip-flops | 10.3.2 |
| | | Resettable latches and flip-flops | 10.3.4 |
| | | Enabled latches and flip-flops 10.3.5 | |
| W | 1 | Interconnect | Chapter 6 |
| | | Wire geometry | 6.1.1 |
| | | Interconnect modeling | 6.2 |
| | | Resistance | 6.2.1 |
| | | Capacitance | 6.2.2 |
| | | Inductance | 6.2.3 |
| | | Skin effect | 6.2.4 |
| | | Delay | 6.3.1 |
| | | Energy | 6.3.2 |
| | | Crosstalk | 6.3.3 |
| | | Interconnect engineering | 6.4 |
| | | Width, spacing, layer | 6.4.1 |
| | | Repeaters | 6.4.2 |
| F | 3 | Arithmetic logic circuits | 11 |
| | | addition | 11.2 |
| M | 6 | Datapath | |
| W | 8 | Design for testability | |
| F | 10 | Packaging | 13.2 |
| | | Power distribution | 13.3 |
| | | Clocks | 13.4 |
| | | Definitions | 13.4.1 |
| | | Clock system architecture | 13.4.2 |
| | | Global clock generation | 13.4.3 |
| | | Global clock distribution | 13.4.4 |
| M | 13 | I/O Pads, ESD, Xmit lines | 13.6 |
| | | Basic I/O pad circuits | 13.6.1 |
| | | Vdd, Vss (Gnd), In, Out | |
| | | Electrostatic discharge protection | 13.6.2 |
| | | Example: MOSIS I/O pad | 13.6.3 |
| | | High speed I/O | 13.7.1 |

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| W | 15 | Power and efficiency | 5.1 |
| | | Dynamic power | 5.2 |
| | | Activity factor | 5.2.1 |
| | | Capacitance | 5.2.2 |
| | | Voltage | 5.2.3 |
| | | Frequency | 5.2.4 |
| | | Short circuit | 5.2.5 |
| | | Static power | 5.3.1 |
| F | 17 | Scaling | 7.4 |
| | | Economics | 14.5 |
| M | 20 | Project progress reports & discussion | |
| W | 22 | SRAM | 12.1-12.2.3 |
| F | 24 | Exam II | |
| M | 27 | Memorial day - no class, work on project | |
| W | 29 | Circuit pitfalls | |
| F | 31 | Project Issues | |
| M June | 3 | CAM, ROM, PLAs | 12.4-12.7 |
| W | 5 | Current issues in VLSI design | |
| F | 7 | Review and wrap-up | |

Wednesday June 12 12:00-1:50pm - Final Exam Time DESIGN REPORTS etc.