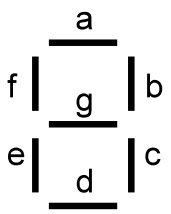
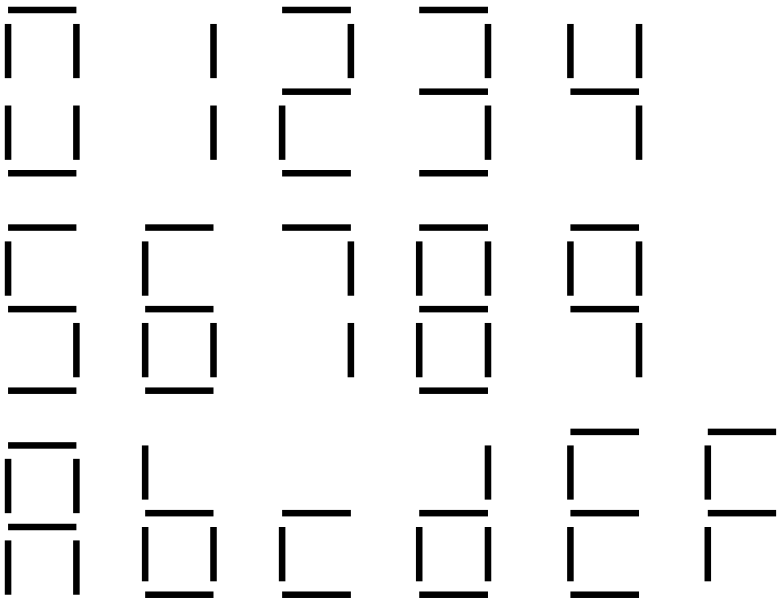
Binary to 7-Segment Decoder ROM

For WWU FPGA boards
Cathodes asserted low

Init value assumes XILINX RAM/ROM component bit ordering.





g	f	e	d	c	b	a	← segment	
0083	308E	02BA	8692	D004	D860	3812	← INIT value	
1	0	0	0	0	0	0	0	
1	1	1	1	0	0	1	1	
0	1	0	0	1	0	0	2	
0	1	1	0	0	0	0	3	
0	0	1	1	0	0	1	4	
0	0	1	0	0	1	0	5	
0	0	0	0	0	1	0	6	
1	1	1	1	0	0	0	7	
0	0	0	0	0	0	0	8	
0	0	1	1	0	0	0	9	
0	0	0	1	0	0	0	10	A
0	0	0	0	0	1	1	11	B
0	1	0	0	1	1	1	12	C
0	1	0	0	0	0	1	13	D
0	0	0	0	1	1	0	14	E
0	0	0	1	1	1	0	15	F