ENGR-435
Topics covered thus far and things to know

Mosfet structure. Key parts of mosfets in an IC
- source, drain, body, gate, channel region, channel length, modes of operation: linear/saturated
- depletion regions, how to build a P-type mosfet on a wafer that starts off as P-doped
- (chapter 5 of Sedra covers some of this)
- know how width and length of the transistor fits into the Ids equation
- as voltage drain to source increases, what happens to Ids.
- if the gate voltage of a mosfet is held constant while the mosfet is operating in saturation, is current Ids constant? if not, why?

CMOS logic circuit topology
- Switch equivalent view of logic circuits
- pull-up & pull-down networks
- NAND, NOR, INV gates
- Complex gates

Inverters
- Vout vs Vin and MOSFET modes of operation as switching occurs
- Noise margin determination & calculation
- Note how Vinput high min & Vinput low max are determined
- Mosfet P and N matching or not matching in the inverter

Dynamic operation of the inverter
- Definition of propagation delay and what it depends on
- Given an equivalent resistance for an N or P type transistor and a load capacitance, know how to approximate the propagation time high-to-low and low-to-high and also the combined propagation time
- Intrinsic capacitances of the Mosfet. We talked about those in class.
- Output capacitances for the inverter. Figure 17.6 shows the key capacitances for one inverter driving another inverter. Q1 and Q2 form the first inverter with its load capacitances shown (gate capacitances of Q3 and Q4 are load capacitances for Q1 and Q2). Note the total affective load capacitance in eq. 17.19

Power dissipation in CMOS circuits
- Static power dissipation (where is static power dissipated in an inverter or NAND gate etc.?)
- Dynamic power dissipation: two main mechanisms
  - periodic charge/discharge of load capacitance (load here includes gate output capac.) know the power dissipation equation
  - short circuit
- power-delay product - know

Pass transistors
- using one N type or one P type transistor to pass a logic 0 or 1 to another circuit is a “good” logic one or a “good” logic zero passed by N and P devices? which one?

What is a transmission gate, its circuit, and its advantage compared to a pass transistor?

How might a master-slave D flip-flop be created?

What is the core (central) circuit of an SRAM memory cell

What is the core circuit of a dynamic (DRAM) memory cell

How is data stored in a flash memory cell? What is its physical structure? How is data read? How is it written to?

Static hazards in logic circuits (not electro-static hazards, although we deal with those too).
    how do we avoid static hazards in say the outputs from a state machine?
    I.e., how to create glitch free signals.

Regarding design of logic circuits, particularly describing designs with VHDL, know how to design a state machine: its register, next-state logic, output logic.
    create state diagrams that have proper, i.e. correct, branching conditions.

I assume you have basic knowledge of VHDL. and I will not be specifically testing your knowledge of VHDL although there could be a question that asks you to create a small piece of circuit using VHDL.