ENGR-435
HW# 6

In class we discussed, and you may have sketched out, a draft block diagram for lab 5. The goal of this homework is for you to finish the block diagram and also create timing information.

General to-do statement

Finish before class:

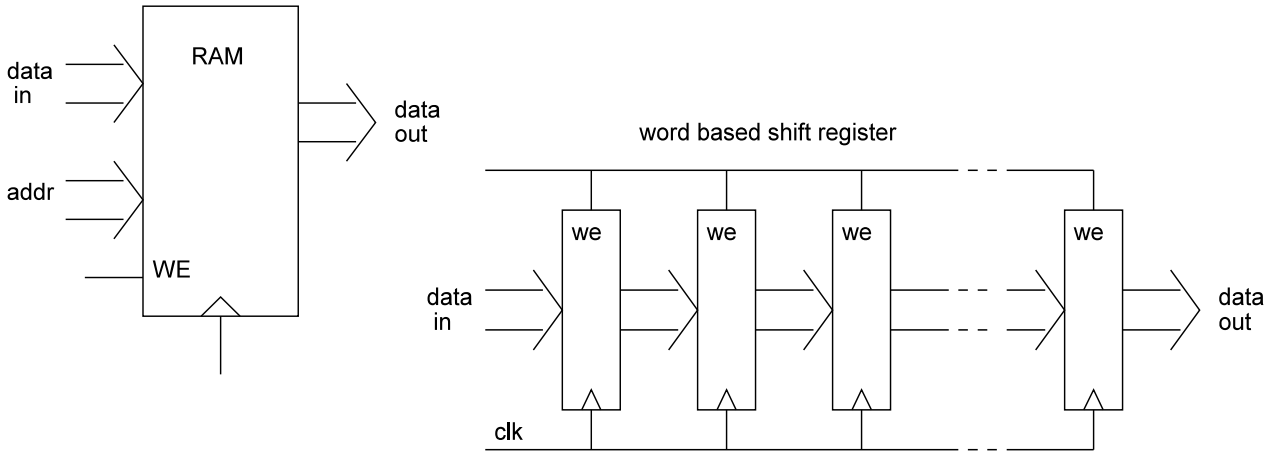
1) your block diagram for the FIR circuit
2) a timing diagram for the FIR circuit
3) **bring (1) and (2) to class Wednesday**

Instructions for this homework

A) The block diagram can be hand drawn (neatly) or drawn with a computer tool.
B) A line on the block diagram that represents multiple signals, i.e. a Bus, should have a short line through it (a slash) with a number alongside indicating how many bits are in it.
C) Arrows at the end of a wire should indicate direction of signal flow
D) The timing diagram does not have to show every clock cycle. In my handout on the ADC I show a timing diagram with each clock transition shown. Clock rates of various signals should be documented but I am not asking you to draw each cycle like I did in my documentation unless it is helpful.
E) Timing documentation should consider that likely the clock that runs the calculation will need to run faster than the clock that paces A/D conversion. Designing with that in mind will also make it easier to increase the number of filter taps in the future if that became desirable.

Memory methods

Two ways of organizing memory are a RAM and a shift register. Below are diagrams of each. The output of the RAM can be asynchronous or synchronous. Input to RAM is synchronous with clock, i.e. if the WriteEnable signal is asserted when a clock edge occurs then input data will be written into the RAM. Writing to the shift register happens on the edge of clock also. Coefficients will come from a ROM.



FIR circuit characteristics and requirements

- The FIR filter will have 32 “taps”, i.e. 32 12-bit data values will be kept and there will be32 12-bit coefficients
- The sample rate, i.e. the rate that new values are captured by the ADC, should be nominally 50Khz.
- Each time the ADC creates a new data word the following calculation is done:

$$R_i = \sum_{k=1}^{n} D_k \times C_k$$

where n = 32, D is data(n), and C is coefficient(n)
Ri is the result

- Each time a new Ri is calculated the possible Ri word size is 24 bits (from multiplying 12 bits times 12 bits) plus 5 more bits from 32 additions totaling 29
- 12 bits out of the possible 29 are chosen to drive the DAC.

Other misc details from the lab handout etc, (some not needed to create a block diagram).

- An analog signal will be digitized using the MCP3201 analog-to-digital convertor (ADC) on the WWU pmod_ad module
- An SPI driver to read data from the ADC is provided for you
- The processed, i.e. digitally filtered, signal will be converted back to analog using the MCP4822 digital-to-analog convertor (DAC) on the WWU pmod_ad module
- The ADC digital output and DAC digital input are both 12 bits
- Analog input voltage range is 0 to 3.3v, thus the analog input signal needs a +1.65v DC component to it or the capacitively coupled (AC) input to the pmod-ad board used
- Digital output voltage range is 0 to 2.04 volts. Thus a zero AC output signal will be 1.02v DC.