Lab Exercise #1

Objective

The objective of this lab is to refresh knowledge of state machine design.

Problem Statement

The On-Top™ elevator company has hired you to design the controls for a new elevator that they are constructing for the A-Ok-Manufacturing™ company. This elevator will be used to send materials between floors in their factory. People will not ride on the elevator. Rather, items will be placed on the elevator and then a button pressed to send the elevator to the desired floor. If the elevator is not at a particular floor and someone on that floor wishes to use the elevator, there will be an elevator call button that will bring it to that floor.

There are two lamps that show when the elevator car is in motion. One illuminates when the car is going up and the other when it is going down (these two lights would be replicated on each floor)

Pressing a Call or a Goto button (on any floor) while the elevator is in motion will have no effect, i.e. it should not change the destination nor create a pending request for motion.

There will be a sensor on each floor that detects when the elevator arrives at and is located at that floor.

Here is a summary of the buttons and sensors for each floor (signal names that are to be used in your design documentation are shown in parenthesis). Recall that on the WWU FPGA3 boards that signals from push buttons are asserted low and signals from switches are asserted high:

			Switch to use
Floor 3 buttons -	Goto 2	(3Go2)	sw8
	Goto 1	(3Go1)	sw7
	Call to 3	(3C3)	sw6
	Floor 3 sensor (S3)		
Floor 2 buttons -	Goto 3	(2Go3)	sw5
	Goto 1	(2Go1)	sw4
	Call to 2	(2C2)	sw3
	Floor 2 sensor (S2)		
Floor 1 buttons -	Goto 3	(1Go3)	sw2
	Goto 2	(1Go2)	sw1
	Call to 1	(1C1)	sw0
	Floor 1 sensor (S1)		

Outputs

Lamps: Two signals, Going up (Lup) or Going down (Ldn) asserted high.
Going up should light LED1 and going down should light LED0

Motor control: There are two signals that must be created to make the elevator move: Motor up (Mup) or Motor down (Mdn) asserted high.

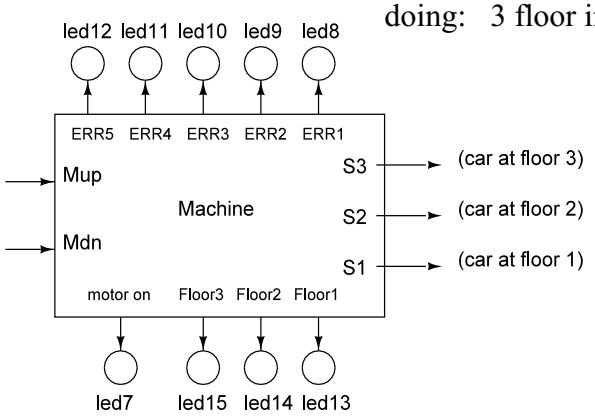
At power up the elevator position will not be known (it may be at a floor or it could be between floors if a power failure has occurred). A reset button should be included that when asserted will cause the elevator to "home" to floor 1.

To emphasize an earlier statement, if the elevator is in motion pressing any call or goto button will have no effect, i.e. there is no queue of pending requests. Also, please use signal names as defined above.

A circuit block called Machine will be used to simulate the elevator itself. This will be supplied to you.

Inputs to Machine are: Mup, Mdn

Outputs from Machine are: S1, S2, S3; also signals intended to show what the elevator is doing: 3 floor indicators, 5 error LEDs, plus a motor-on LED.



The floor indicators Floor1 etc. are signals S1, S2, S3.

ERR1 at floor1, Mdn asserted
ERR2 at floor1, Mdn & Mup asserted
ERR3 at floor2, Mdn & Mup asserted
ERR4 at floor3, Mdn & Mup asserted
ERR5 at floor3, Mup asserted

Design

Each person is to design an elevator controller. A state machine is expected to be a significant functional block in this design. You need to create a well labeled state diagram and a block diagram of the system.

Implementation

Your design is to be implemented on a WWU FPGA3 board. Use VHDL to describe your design.

To Turn In

Each person will submit a design that consists of a well labeled state diagram, a block diagram of the system including the state machine, any notes needed to support the design, a screen shot of the design summary in ISE, and your VHDL description (in your VHDL file, state if the design is for an FPGA board with DRAM or DDR3 memory). The audience for your design documents is a person, a peer, who knows how to implement the logic for a state machine etc but does not know the particulars of the problem statement. You may submit the report to D2L or hand in a paper version, your choice. In either case, upload your .bit file to D2L.