Lab Exercise #2

ENGR-435

Objectivess

- Review design of digital systems that incorporate state machines, counters, multiplexers, etc.
- Gain further experience using VHDL
- Design a system with memory elements all clocked by the master clock but with update rate regulated with enables.

References

Xilinx documents on the class web page.
Pinout for the WWU FPGA3 digital logic board (found on the class webpage)

Problem Statement

Design a "stop watch" circuit that will measure time up to 99 seconds in hundredths of seconds and display the measured time in 4 decimal digits, two for seconds, two for hundredths. There will be two buttons used to operate the stop watch. Button one will be pressed to start time and pressed a second time to stop time. Button two will be used to reset time to zero once counting has stopped. Button three button will allow display of lap time, i.e. pressing the third button will freeze the current time on the display while allowing the counters to continue running and measure the total elapsed time. Pressing this third button a second time will cause the display to revert to "running" time. Time is to be displayed in base 10 on a 7-segment display that has 4 digits plus a colon to denote separation between seconds and fractions of seconds. Use a state machine to monitor the buttons and assert control signals needed by the counter(s). Flip-flop and register clock inputs shall all be connected to mclk. Use enables to control when memory elements are able to up date.

Design Flow

The general design flow for today's lab is:

- Design a circuit per the problem statement.
  - Confirm understanding of the problem & partition the design into subsystems.
  - Create a block diagram(s) and fully documented state diagram(s) as needed.
  - Create a timing diagram showing timing for key parts of the circuit.
  - Write a VHDL description of your circuit
  - Compile and confirm syntax correctness
- (Implement the design)
  - Synthesize an FPGA implementation (Place, route, and create a bit map file)
  - Download bit map file to the FPGA board
  - Test (debug if needed)

Specific input/output resources to use:

sw11 will be the main button, i.e. the start/stop button
sw10 will be the reset switch
sw13 will be the lap button
display will be on the 7-segment display

Suggestion to aid debugging

Because you cannot connect a scope probe onto circuit nodes inside an FPGA, bring out signals that could be useful for debugging using the ExtOut or TEK signal lines where a scope can be connected. If signals change slowly enough, connect signals to LEDs to observe them.

To Turn In

- By next lab period, a short report containing:
  1) A page that has an abstract on it (one paragraph, see below)
  1a) A page with comments about any problems encountered, things learned, etc.
  2) Block diagram**
  3) VHDL description, i.e. your .vhd file
  4) Screen shot of the ISE design summary screen
  5) Submit .vhd and .ucf files to D2L drop box
  6) The report can be submitted on paper or submitted via D2L

What is an abstract?

An abstract typically is one paragraph that is written concisely to summarize what was done, how the problem or project was approached, possibly what materials were used, and what resulted from the effort including a clear statement about it meeting design goals (i.e., did it work). Consider it written to peers, i.e. people who know in general about digital circuits but who are not familiar with your project.

** The block diagram can be hand drawn and scanned or photographed so long as the contrast is good and thus easily readable. Also, it must be neatly drawn with easily read lettering.