ENGR-435 - Lab Excercise # 3

Design of an interface to a MCP-4822 DAC

Goal: To design a circuit that will accept a 12bit data word and send it serially to a Microchip MCP-4822 D/A converter chip.

The target hardware will be a WWU Pmod_ad1 board on which is an MCP4822 chip. This board will be connected to a WWU fpga3 board using its Pmod1 connector. The WWU fpga3 board will be equipped with a Xilinx Spartan-6 FPGA.

VHDL will be used to describe your design. Your circuit will have these inputs and outputs:

Inputs (in a target system coming from another function block. In testing, switches)
- Master clock (50 Mhz)
- a 12 bit data word
- a one bit signal to specify which D/A channel is to be loaded. 0=A and 1=B

Outputs (going to the DAC)
- Chip select (asserted low)
- Serial data
- Load (asserted low)
- Serial clock

Design approach

Create a block diagram of your circuit, state diagrams for any state machines, and possibly a timing diagram(s). Then write a VHDL description. Synthesize. Download and test on the FPGA board.

Connect 12 toggle switches or buttons as input to your circuit for testing (I suggest using toggle switches as the most significant bits). Measure the analog output with a voltmeter and/or oscilloscope.

To turn in

The documentation you create in doing your design and the VHDL file you create. At the top of the VHDL file place a description of circuit function or malfunction depending on the state of your lab when you submit it. Also, after synthesizing your final version submit a screen shot of ISE with the design summary window showing.

Notes:

1) A reasonable question is: how fast does the SCK signal to the D/A need to be. The data sheet shows 20Mhz to be max. But we may not need to run that fast. Assume that we wish to send out audio with a good frequency range. Commercial CDs use a 44.1 Khz sample rate. This means that 44.1Khz times per second a new complete word of data is used. At least 16 bits of data have to be transferred to the DAC for each data item. So for one channel SCK has to be at least 16x44.1Khz or 705.6 Khz. That would be the slowest clock to use. 50 Mhz / 705.6 Khz means divide by 70.86. Rounding down to a near power of two would be 64. That is a reasonable rate for this assignment. A little faster clock, such as 1 Mhz would give a little time between sending one data word and the next.