Lab Exercise #4

Objectivess

- Gain further experience designing digital systems using VHDL .
- Create a digital waveform generator whose output will drive the D/A converter to create musical tones
- Have some fun

References

Xilinx documents on the class web page.
Pinout for the WWU FPGA3 digital logic board (found on the class webpage)

Problem Statement

Create a circuit that will generate the notes needed to play a simple song such as Mary Had a Little Lamb. Buttons on the FPGA3 board will be assigned to create different notes allowing a user to play a song.

Implement a direct digital frequency synthesis (DDFS) circuit to create the needed notes.

Design Flow

The general design flow for today's lab is:
- Design a circuit per the problem statement.
    Confirm understanding of the problem & partition the design into subsystems.
    Create a block diagram
    As needed, create state diagrams.
    Write VHDL statements to describe the circuit
- Synthesize an FPGA implementation (Place, route, and create a bit map file)
- Download bit map file to the FPGA board
- Test (debug if needed)

Specific input/output resources to use:
    sw9 will select C5 (high C 523.25 Hz   fcw=11237)
    sw10 will select A4 (440.00 Hz fcw=9449)
    sw11 will select G4 (392.00 Hz fcw=8418)
    sw12 will select F4 (349.23 Hz   fcw=7500)
    DAC channel A (or B if you wish) will be the analog output.

    Connect the MSB of the phase register to EXTOUT(0) for monitoring

Suggestion to aid debugging

Because you cannot connect a scope probe onto circuit nodes inside an FPGA, bring out signals that would be useful for debugging using the ExtOut or Tek signal lines where a scope or logic analyzer can be connected. If signals change slowly enough connect signals to LEDs to observe them. Monitor the analog output with the scope.

To Turn In

  - By next lab period, a short report containing:
    - > Abstract (which includes a statement about results), block diagram, summary statement commenting on any problems encountered, things learned, etc.
    - > VHDL file, .bit file