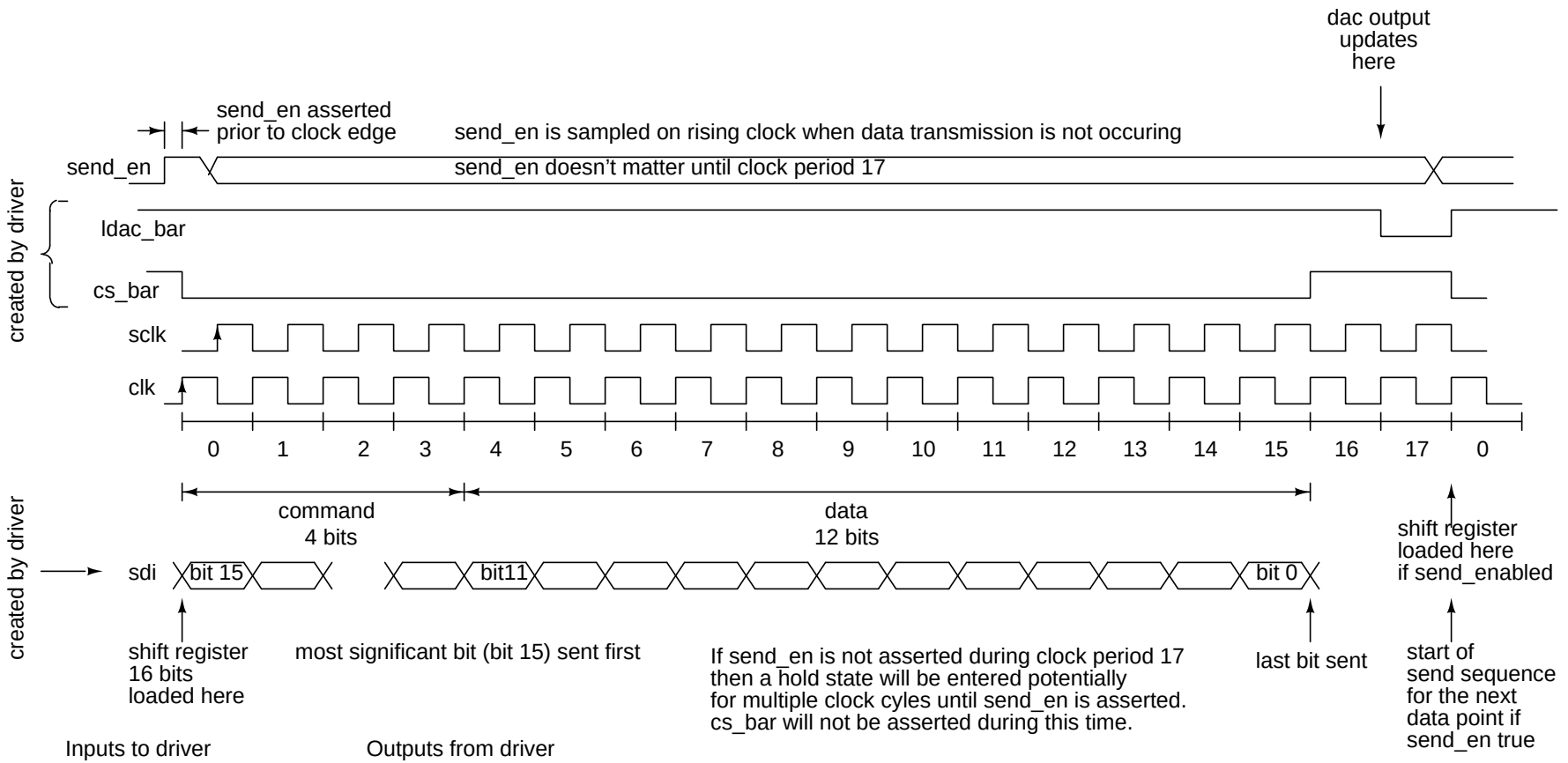

Inputs to driver

- clk
- send_en
- dac_data (12 bits)

Outputs from driver

- ldac_bar
- cs_bar
- sdi

(sclk is $\overline{clk}$)

Timing sequence driving a Microchip MCP4822 DAC

WWU Pmod A/D - D/A Board		
dac_driver_ip.vhd timing diagram		
L.Aamodt		5/23/21