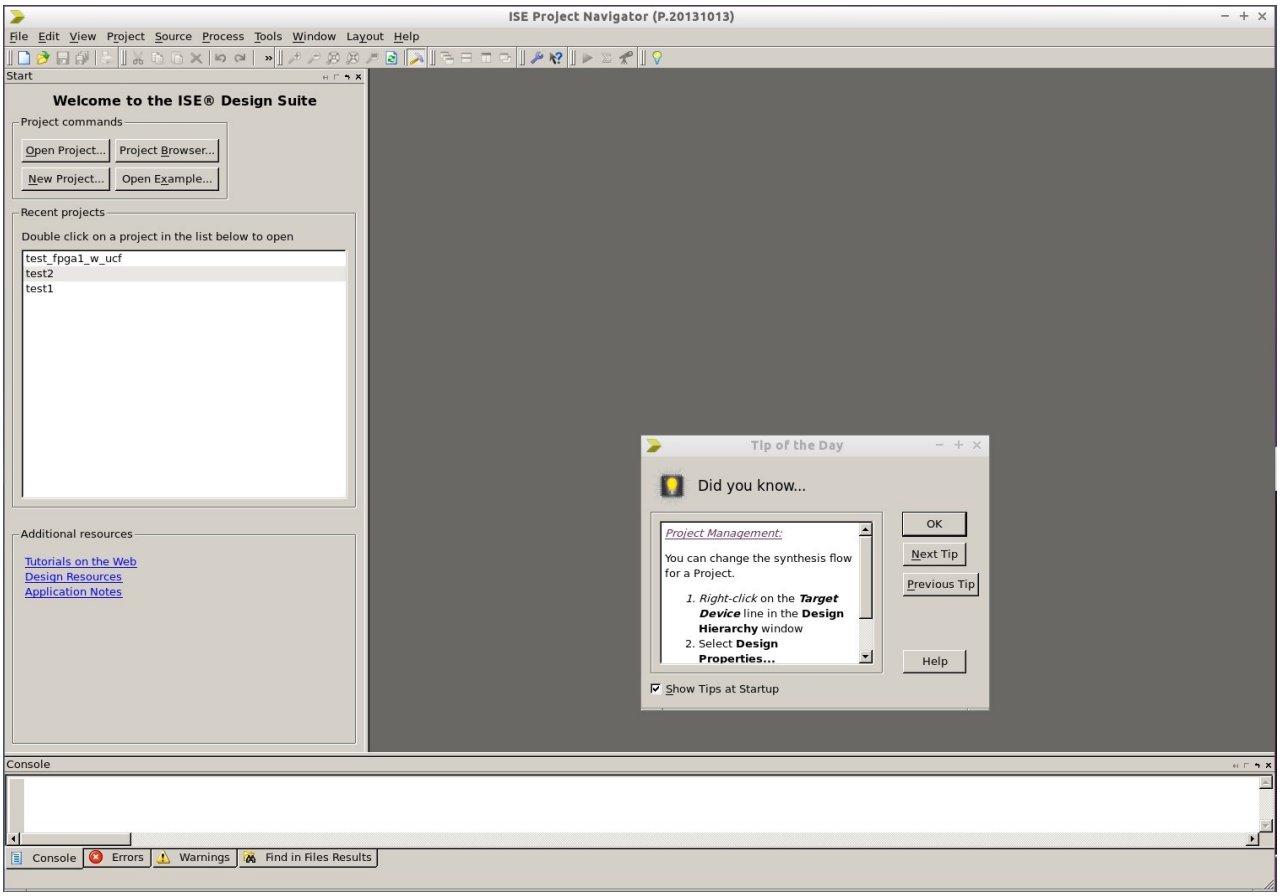
Xilinx Tool Introduction
Getting Started - Schematic Based
rev 10/04/18

0) Create a directory (folder) for a new design. Open a terminal window and make the new folder the current directory:
Use the cd nnnnn command, where nnnnn is the name of the newly created directory..

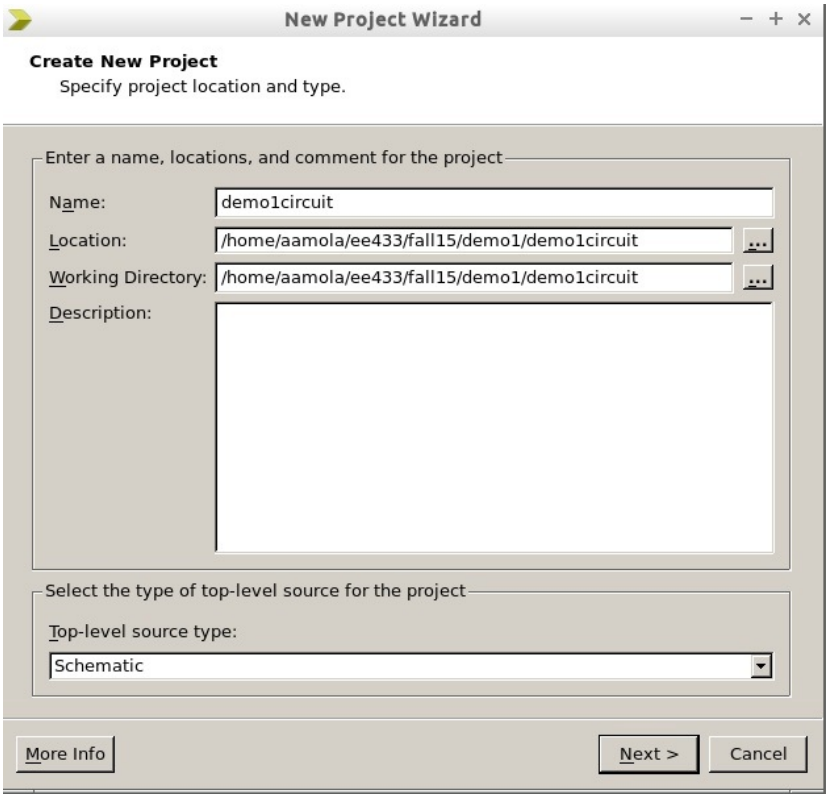
1) Start the Xilinx 14 ISE software by entering **ise** in the terminal window and pressing enter (note the command is lower case).
ISE may start up with a prior design loaded. If so, click **File** on the tool bar and select **close**.
You can also click OK in the Tip-Of-The-Day window.



2) In the upper left four “buttons” will be displayed.

Create a new project by clicking on the **New Project**. button

a) A *New Project Wizard* pop-up window will open. The path to a prior project may be shown. Before entering the name of a new project, select the directory (folder) where the new project will be created. Click the little box with dots (...) to the right of the **Location** field and navigate to the desired directory (folder) where you wish to place your design.

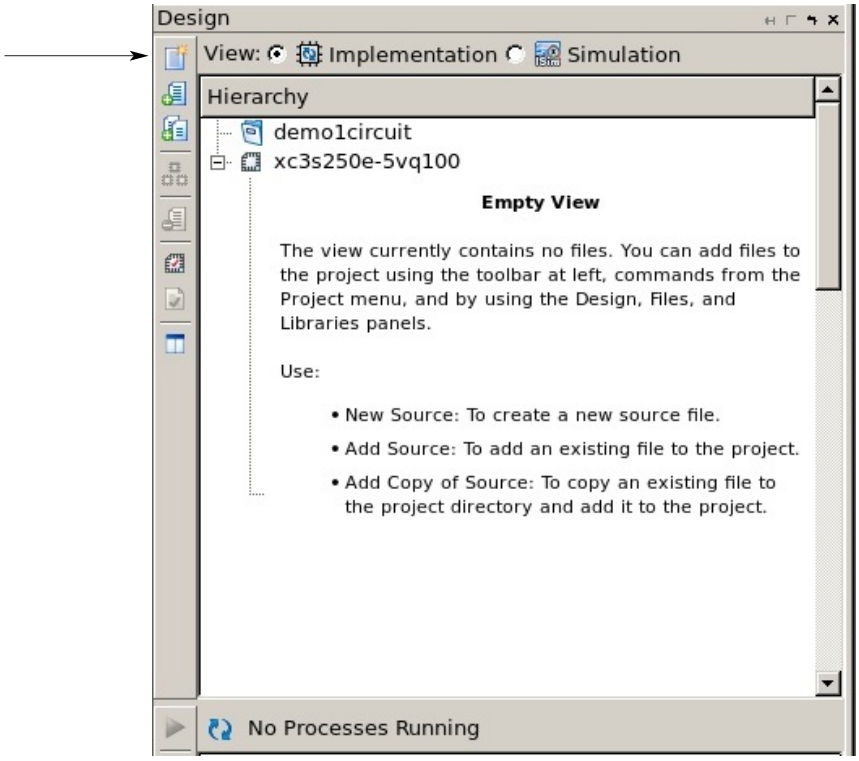


b) Type in a project name (it will show up in the Location field also as you type)
c) Select Schematic as the type of top-level source for the project.
d) Click **Next**
e) The *Project Settings* screen should appear. Set it up as follows:

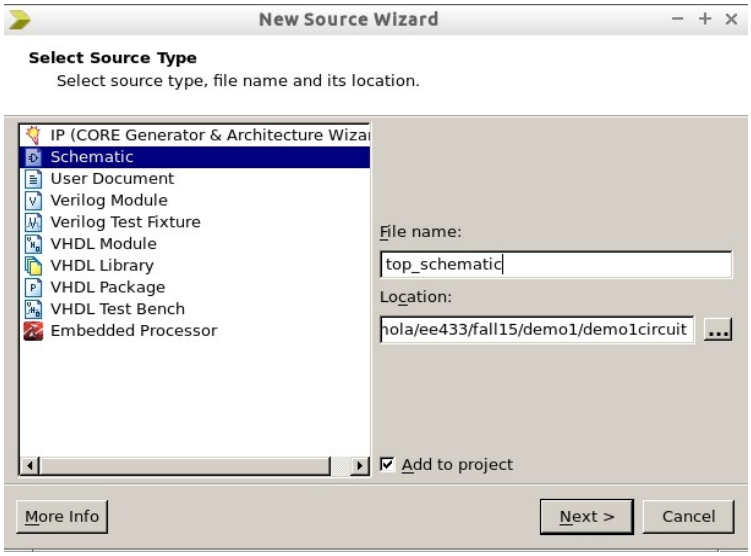
Evaluation Dev Board	None specified
Product Category	General Purpose
Family	Spartan3E
Device	XC3S1200E
Package	FT256
Speed	-5
Top-level Source Type	Schematic (this field may be grayed out. Thats ok)
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property specification	Store all values

f) Click **Next**
g) The *Project Summary* screen should appear. Look over the information. If something is not as you desire then use the **Back** button to go back and make a correction. Otherwise click **Finish**.

h) In the upper left of the screen is a box with the words Hierarchy at the top. Just left of that are a row of iconic buttons. The top icon is New Source. Click on it.

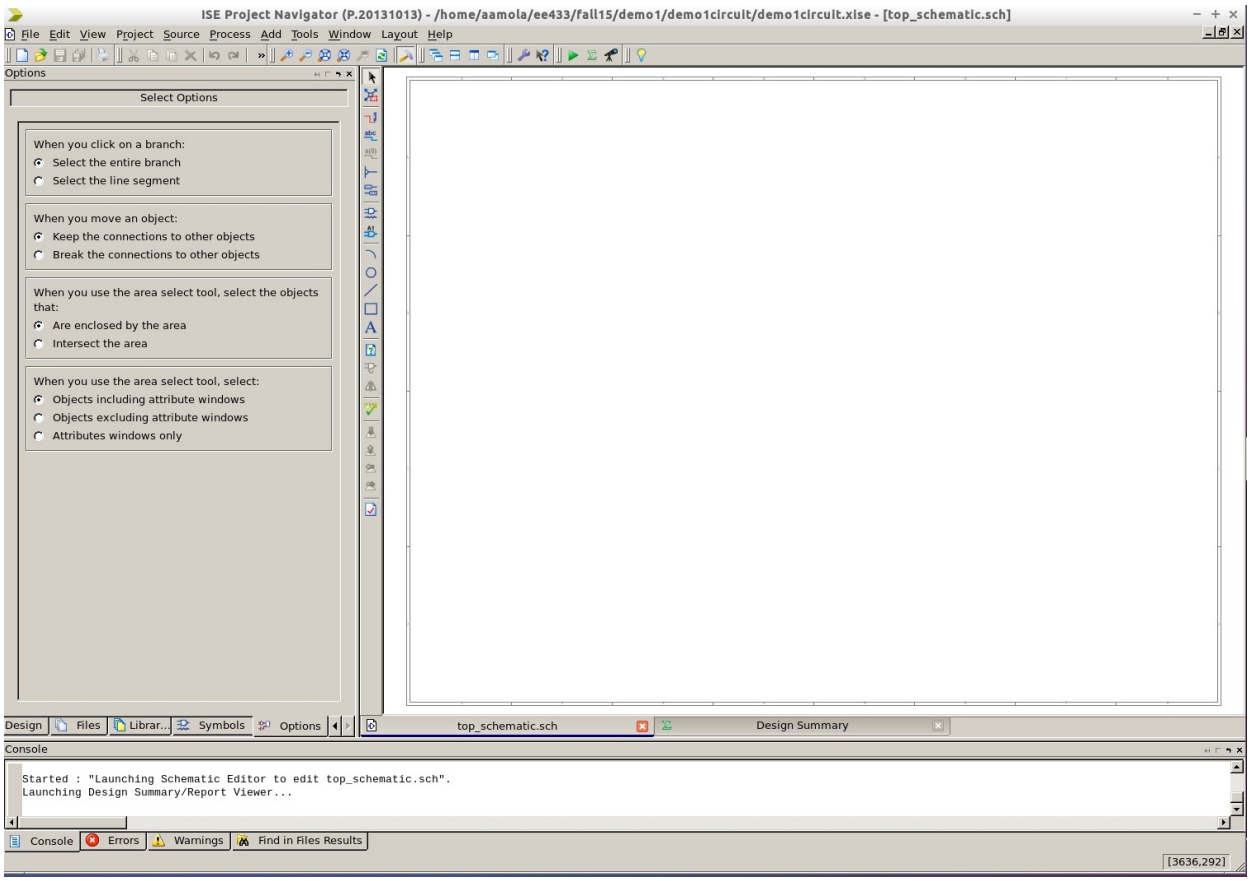


i) The *Create New Source* wizard window should appear. Click on **Schematic** and then type in a file name. I suggest using **top_sch_pname** where pname is a name associate with your project (in the example shown I just use top_schematic but you can do better). Since designs can be created hierarchically this naming convention will make clear that this is the highest level of your design and is a schematic type design block. Click **Next**. The *New Source Wizard Summary* will be displayed. Click **Finish**.



You may be told that the directory xxx/nnnnn (xxx represents a path string) does not exist, would you like to create it? Answer yes.

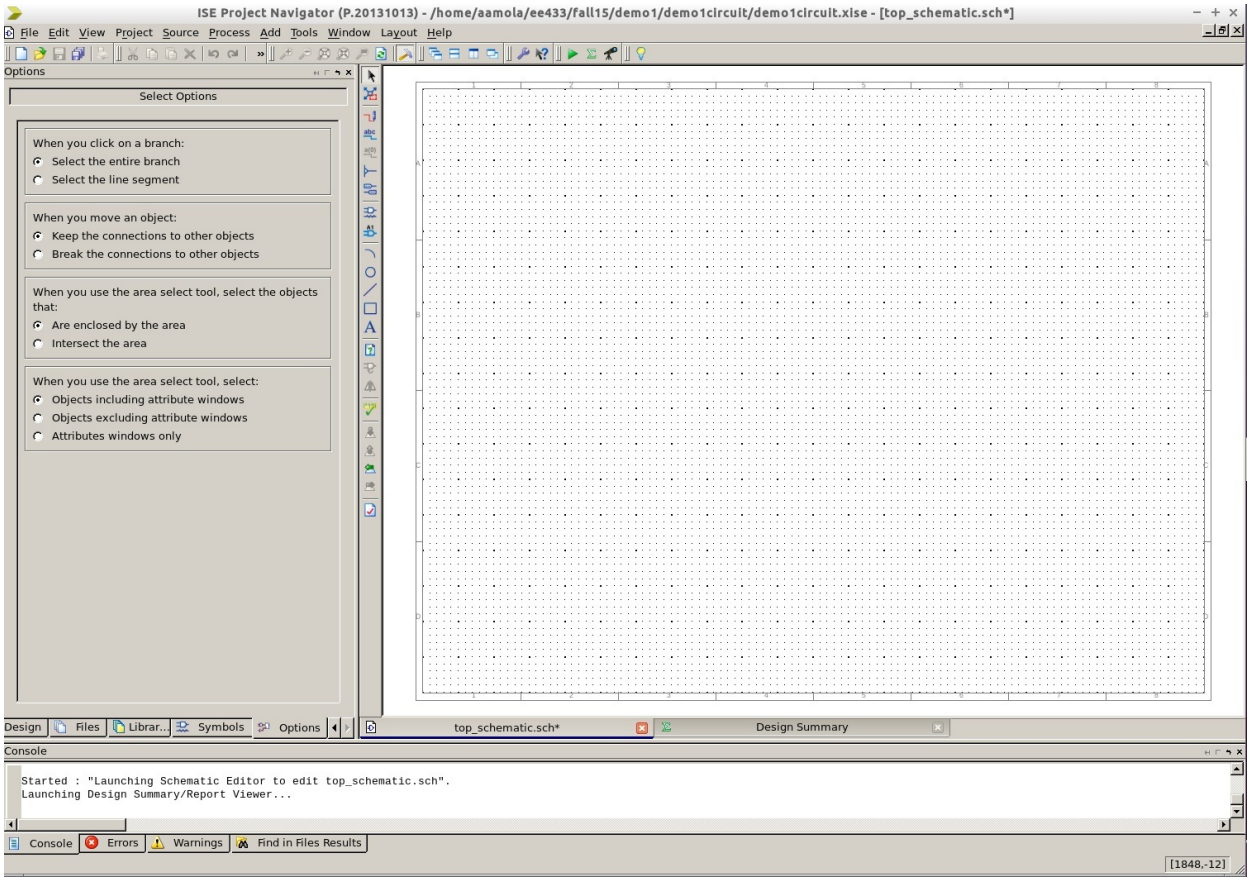
3) A blank schematic sheet should appear in the right 2/3 of the ISE window.
And on the left you should see a subwindow with several tabs at the bottom. Tabs include Design, Files, Library, Symbols, Options.



a) Right click on the schematic in the right window and then click Object Properties at the bottom of the pop-up menu. A sheet size of 22x17 (C size) will be shown. Click on **C=22x17** below size which should open a list of sheet sizes. For your first simple design click on **A=11x8.5** and then click **OK**.

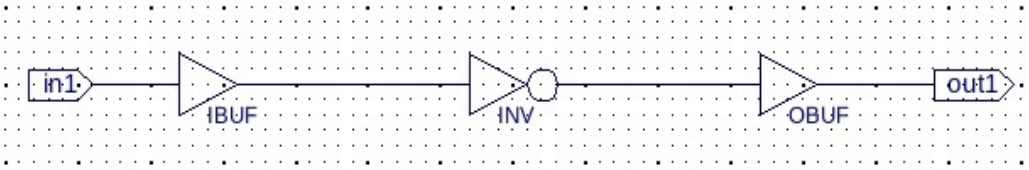
Note 1: For designs larger than the initial test design you likely will wish to use a B or C size sheet.

(after changing sheet size to A the screen likely will show a grid of dots)



4) The goal now is to create a simple circuit. The circuit will be a signal coming in to an invertor and then going out again. Three circuit components (ibuf, inv, obuf) and two connectivity symbols for specifying connections to the outside world will be required.
   a) Click on the Symbols tab at the bottom of the left subwindow. Two smaller windows should open with the top labeled *Categories* and the lower *Symbols*.
   b) Click on category **General** and symbol **Title**. Move the cursor right and a title block will move over the schematic sheet. Move it towards the lower right corner of the sheet and click. Hit the Escape key to unconnect the cursor from the symbol. Then grab the top edge of the title block by positioning the cursor over it and holding down the left mouse button. Move the symbol tight into the lower right corner of the sheet and release. XILINX will be displayed in the title block but that can be edited. More on that later.

(here is the finished circuit)

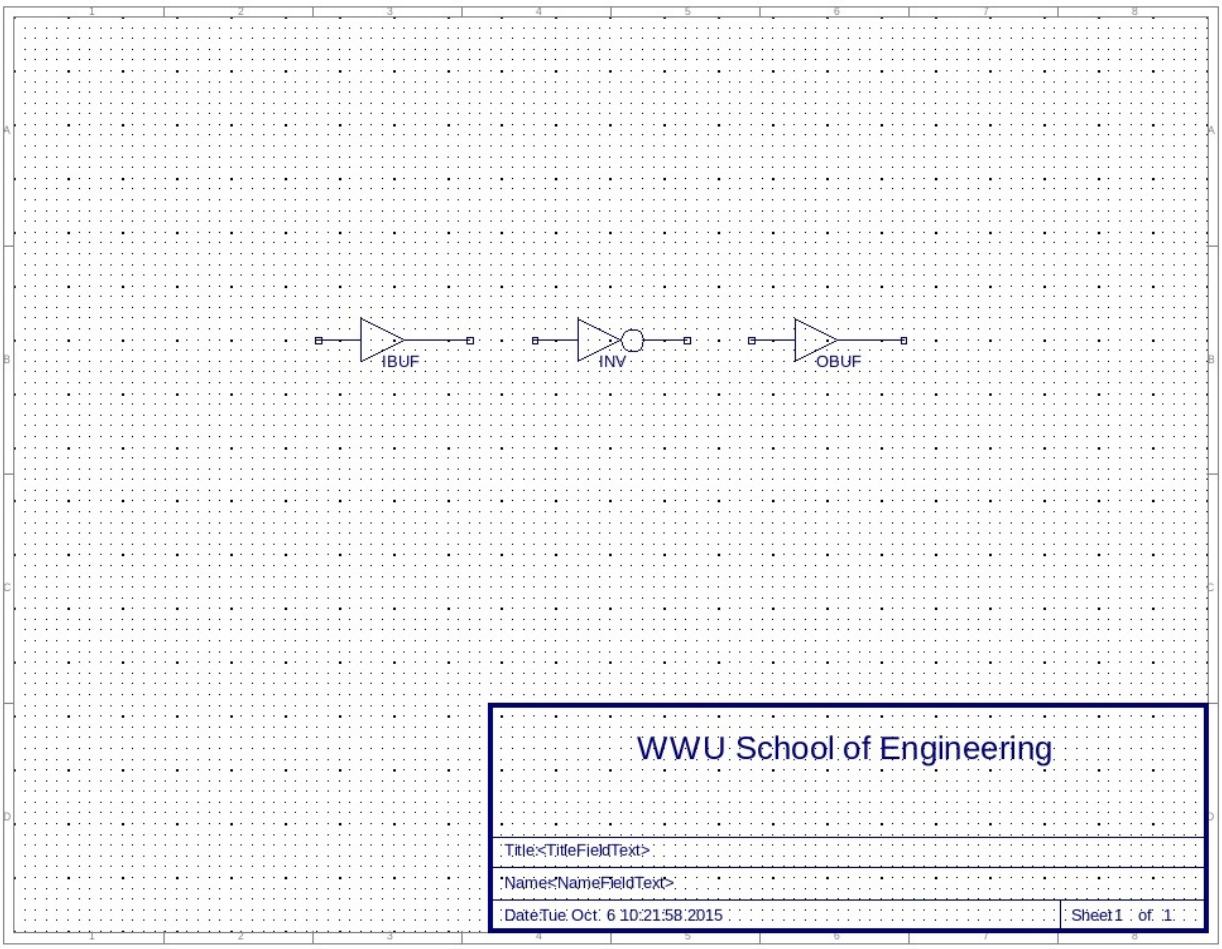


Place circuit components on the schematic.

c) In the *Categories* window click on **I/O** (scroll if needed). Then find **ibuf** (input buffer) in the *Symbols* window below and click it. Move your cursor to a location toward the left of the schematic sheet and centered vertically above the title block. Click once.

d) Repeat for **obuf** placing it horizontally aligned with ibuf but to the right on the sheet.

e) In the *Categories* window select **Logic** and in the *Symbols* window find **inv** and place between ibuf and obuf.



Next the inverter needs to be wired to the input and output buffers.

d) Along the left edge of the schematic window is a Tool bar. The third icon down is the Add Wire tool. Select that.. On the schematic, single left click at the point to start a wire and single left click where you wish it to end.

Next an I/O marker must be added to the ibuf input and obuf output.

e) On the tool bar at schematic left, select Add I/O Marker (7^{th} icon down). Left click on the end of the wire going into the ibuf. Then left click on the end of the wire coming out of the obuf. The I/O marker symbols will have an auto generated name in them.

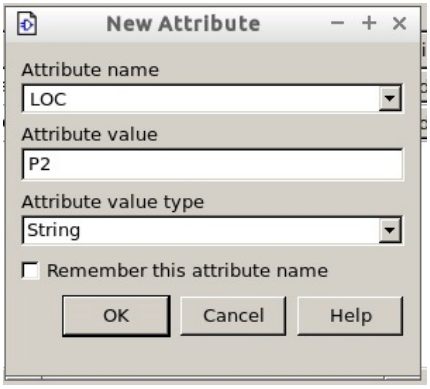
Attributes of the I/O markers need to be changed to identify the physical pin on the FPGA that they are associated with and the marker name can be changed to reflect the signal name. Pin numbers start with capital letter such as H14 etc.

f) Right click on the I/O marker and a pop-up menu will appear. Click on **Object Properties**. An Object Properties window will open. On the left under Category click on **Nets**. Towards the right of the window click on the **New** button. A New Attribute window will open with the default attribute name of LOC. For Attribute Name type in a pin number (has to start with a capital letter). Click OK. [R16 is switch 0]

   Default net names start with XLXN which is cryptic. Change the value of the Name attribute to reflect the signal on that net. For example, in1, out1, or sw0, led0, etc (don't use spaces in net names). Then click OK.

g) Repeat for other I/O markers. For example, the output might be for LED #0.

(See handout, available on the class web page, defining FPGA pinout & function).



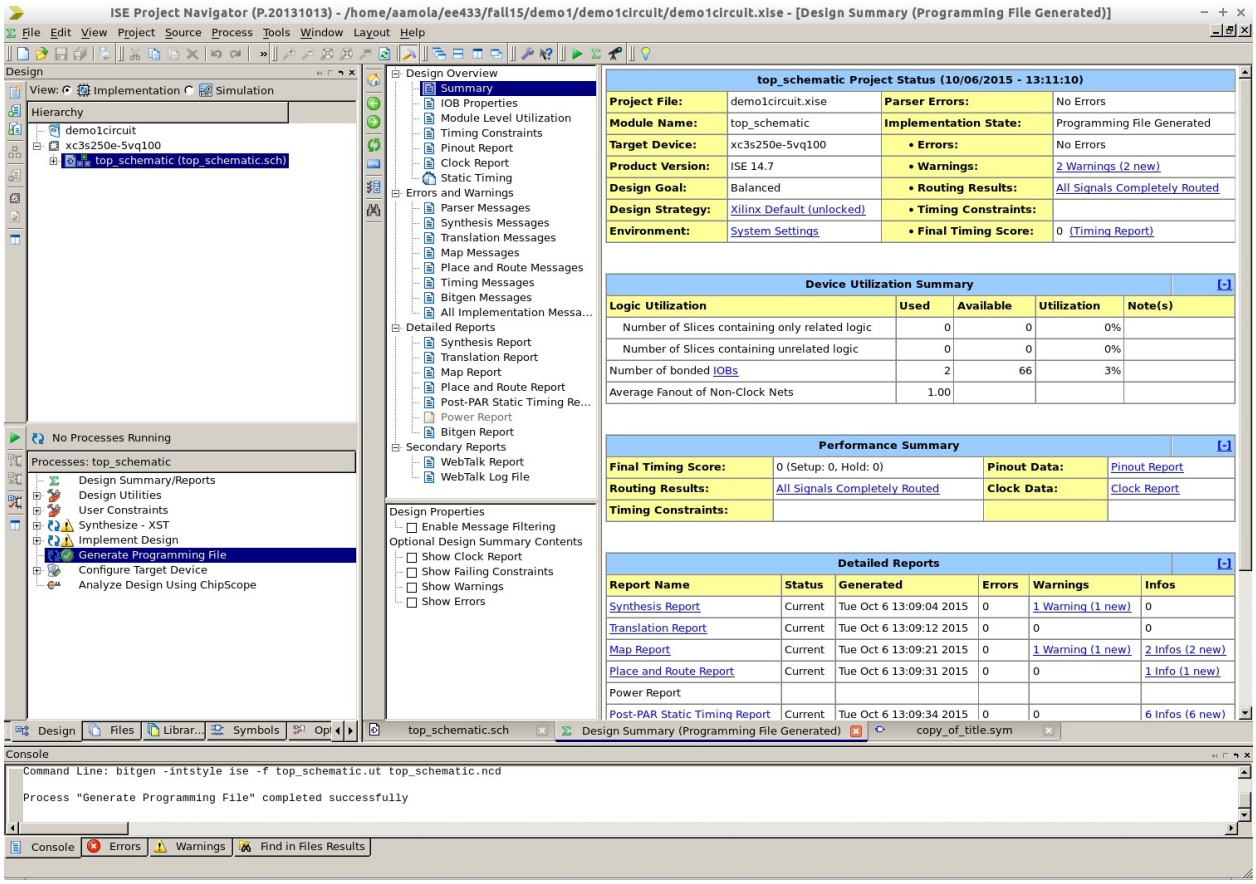
5) When all parts are added and wired up you can do what is called Design Rule Check (DRC) of the schematic. This check does not tell you that the circuit will work, only that signals are connected to component inputs, etc. Messages from the DRC check are displayed in the transcript window at the bottom of the screen. DRC knows nothing about what your circuit is suppose to do.
   a) From the tool bar at the left of the schematic click on the check mark symbol, 6th up from the bottom.

6) The time has come to synthesize the FPGA configuration information from the schematic you have entered.
   a) First, set up display of useful information. Under the schematic click the tab labeled **Design Summary**. Then from the lower left tabs click on **Design**.
   b) Then on the horizontal tool bar at the top is a green arrow symbol., the **Implement Top Module button**. Left click the green arrow.

      It may ask if you wish to save changes. If you don't save it will use the design as it was prior to your last edit. The Implement step will take some time. Be patient. There can be several seconds delay from when you click and when new info appears on the screen while program code is downloaded from the server and run. There are several different programs that run. Information will scroll by in the transcript window if it is open and the Design Summary window will update.

      Watch the sequence of results as synthesis, place, and route occur.

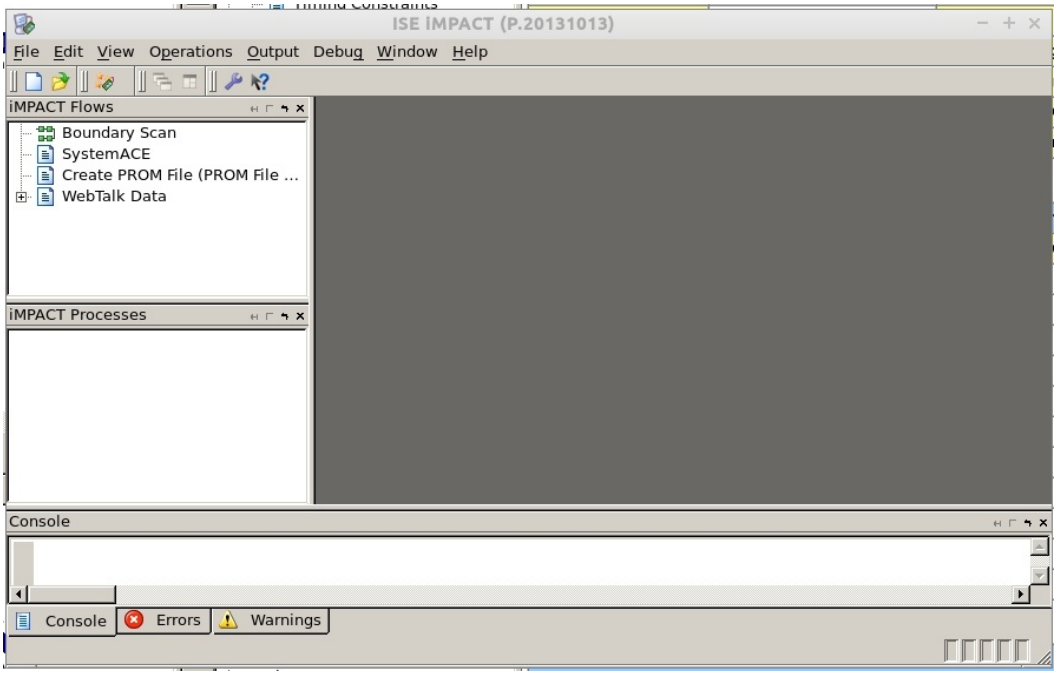
c) Next, in the lower left window double click **Generate Programming File** to generate the bit map file that will be downloaded to configure the FPGA



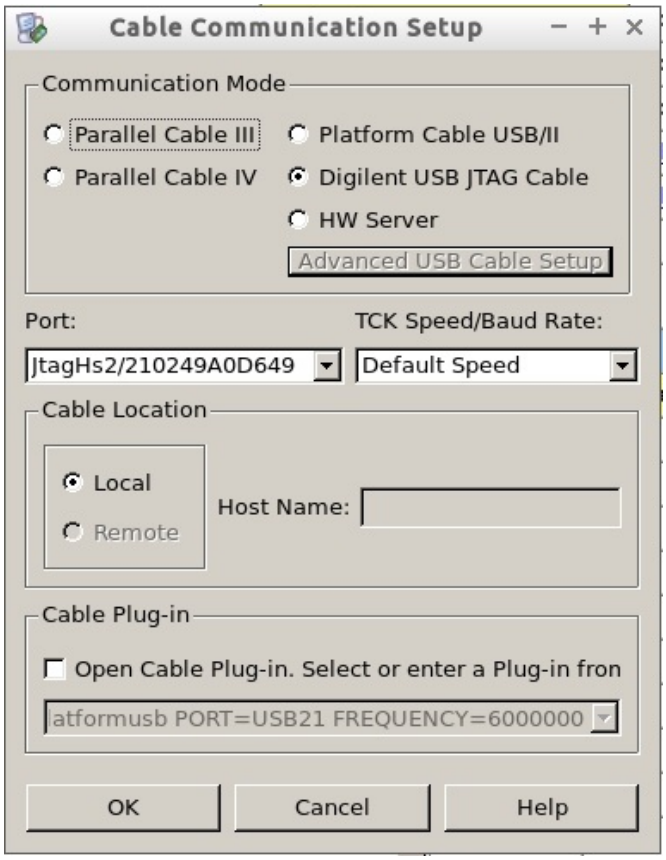
7) Downloading the design to the FPGA
At this point make sure that the programming cable is connected between computer and FPGA board and then apply power to the FPGA board.

Double click **Configure Target Device** to start the iMPACT program. A Project Navigator window may open warning that no iMPACT project file exists. Click **OK**.

The initial screen may look like this:

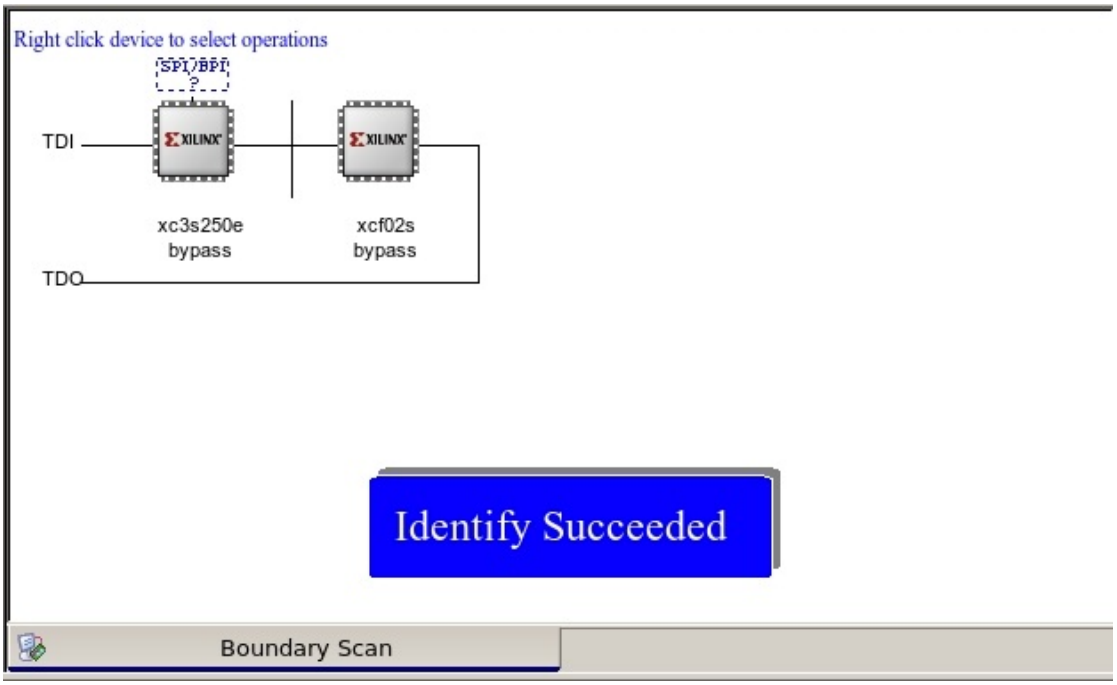


Double click on Boundary Scan. The larger area to the right should turn white with a message “Right click to select device ....”. Right click and in the pop-up box that appears select Cable Setup. The cable setup box looks like this:



If not already selected, **select Digilent USB JTAG Cable**. **Click OK.**

Again right click on the large white window to the right and select Initialize Chain. The right window should look something like this:



A pop box will ask this:

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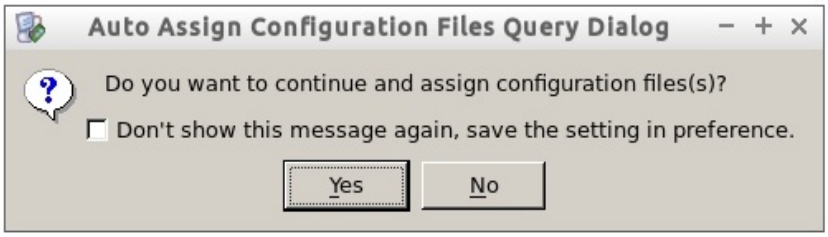
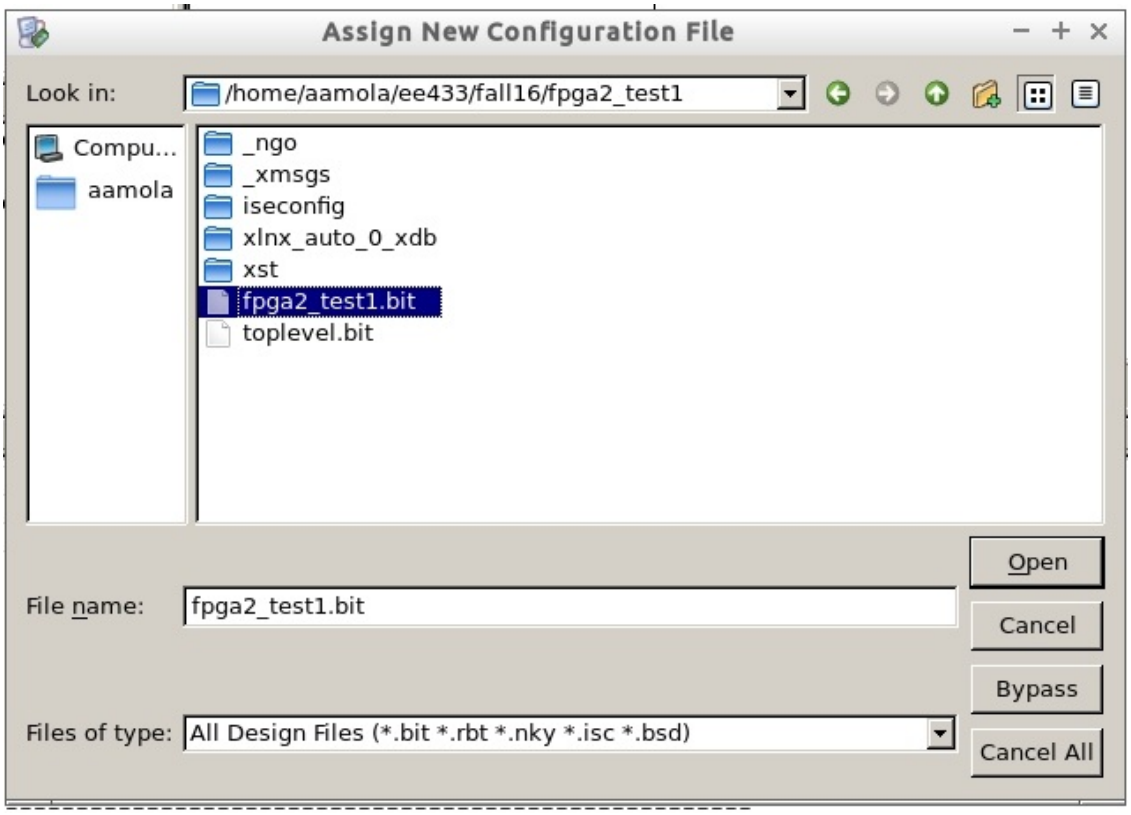
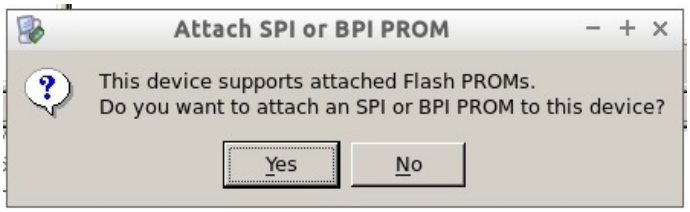


Click Yes. Configuration filenames have a .bit extension. Navigate if needed to the correct directory where your .bit file is located.

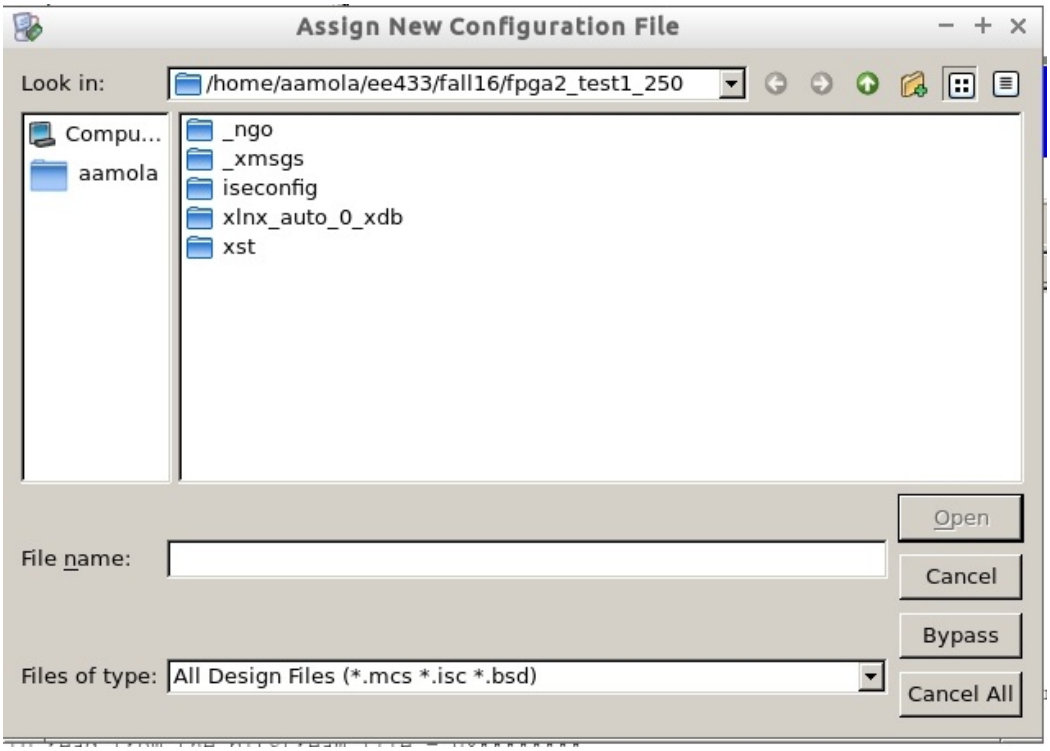


Because there is a second part on the FPGA board a window like this may appear:

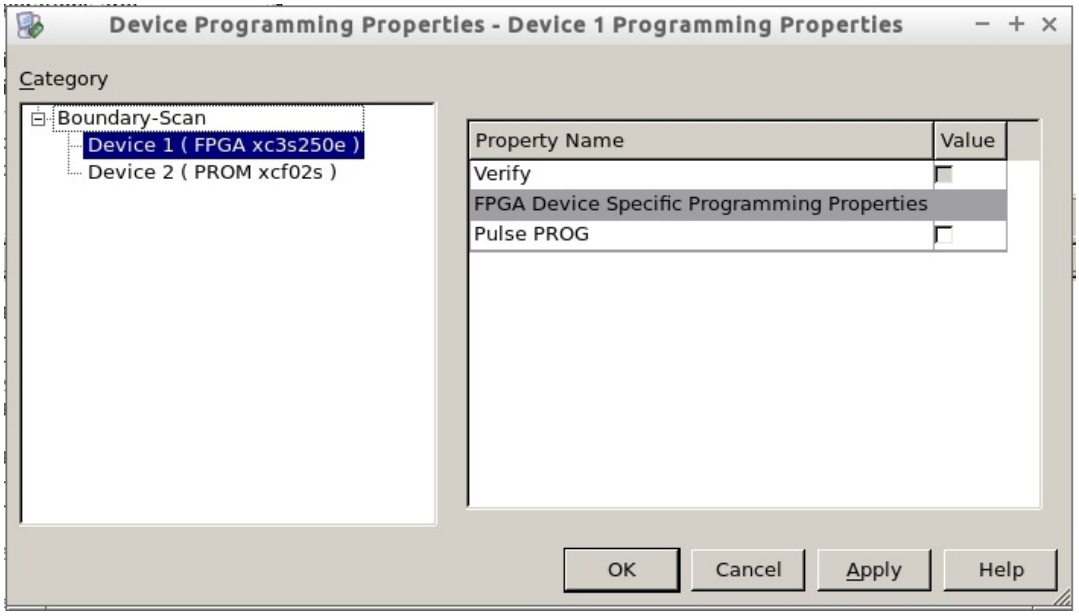


Click No. (you don't want to down load to the PROM memory chip)

Even though you said No to attaching the SPI memory part a window like this may open as if to allow selection of a data file to be downloaded to memory. **Click Bypass**:



The next window is titled Device Programming Properties. It may state that there are no applicable properties for this device. Just click **OK**.



Believe it or not you are now ready to download the .bit file to the FPGA. In the lower left window double click Program. Or right click on the FPGA in the right window.

Before exiting iMPACT I recommend that you do a cable disconnect under *Output* on the tool bar (Disconnect All Cables).